OKI Semiconductor

MSM82C51A-2RS/GS/JS

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

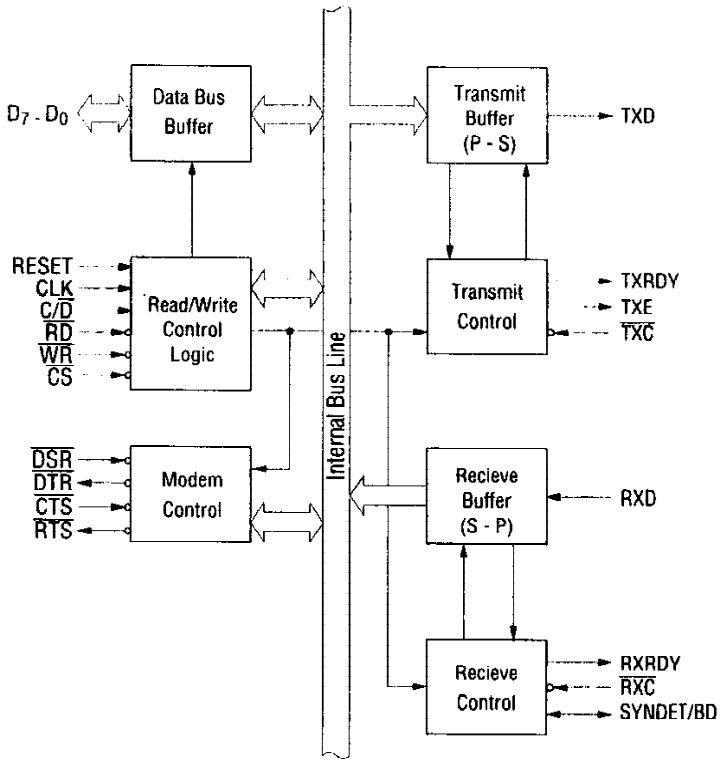
GENERAL DESCRIPTION

The MSM82C51A-2 is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.
As a peripheral device of a microcomputer system, the MSM82C51A-2 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.
The MSM82C51A-2 configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on extremely low power at 100 μA (max) of standby current by suspending all operations.

FEATURES

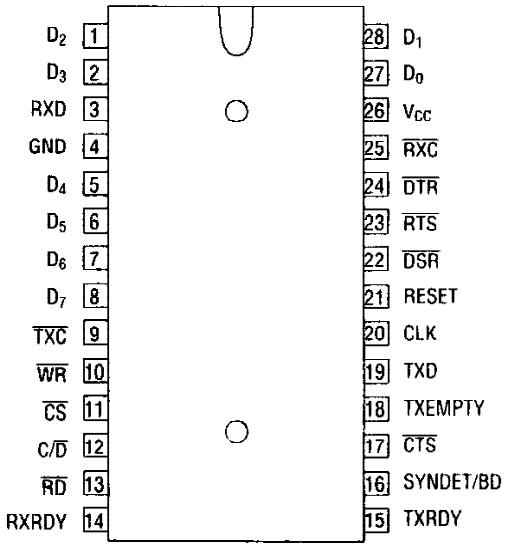
- Wide power supply voltage range from 3 V to 6 V
- Wide temperature range from –40°C to 85°C
- Synchronous communication upto 64 Kbaud
- Asynchronous communication upto 38.4 Kbaud
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin Plastic DIP (DIP28-P-600): MSM82C51A-2RS
- 28-pin Plastic QFJ (QFJ28-P-S450): MSM82C51A-2JS
- 32-pin Plastic SOP(SSOP32-P-430-K): MSM82C51A-2GS-K

FUNCTIONAL BLOCK DIAGRAM

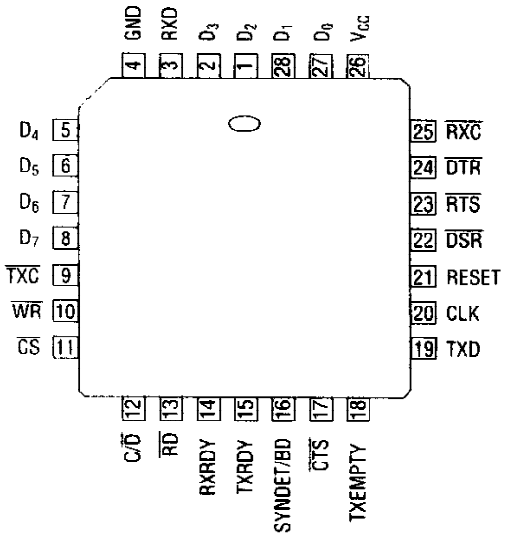


PIN CONFIGURATION (TOP VIEW)

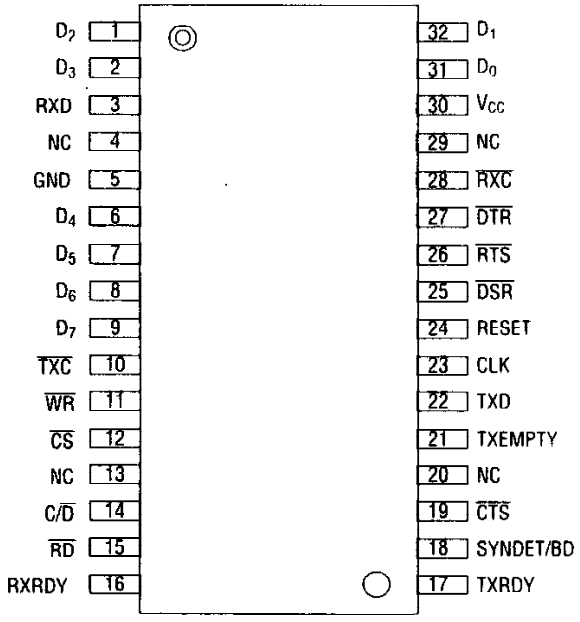
28 pin Plastic DIP



28 pin Plastic QFJ



32 pin Plastic SSOP



FUNCTION

Outline

The MSM82C51A-2's functional configuration is programed by software.
Operation between the MSM82C51A-2 and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

Table 1 Operation between MSM82C51A and CPU

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting the MSM82C51A-2. Fig. 1 shows the function-setting sequence.
If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

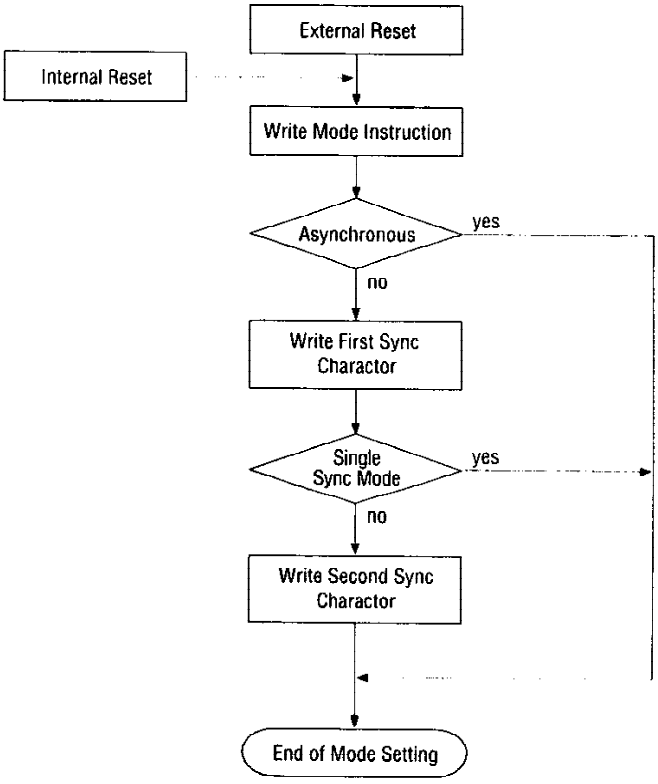


Fig. 1 Function-setting Sequence (Mode Instruction Sequence)

Control Words

There are two types of control word.
1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the MSM82C51A-2. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."
Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one-or two byte sync characters.
If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

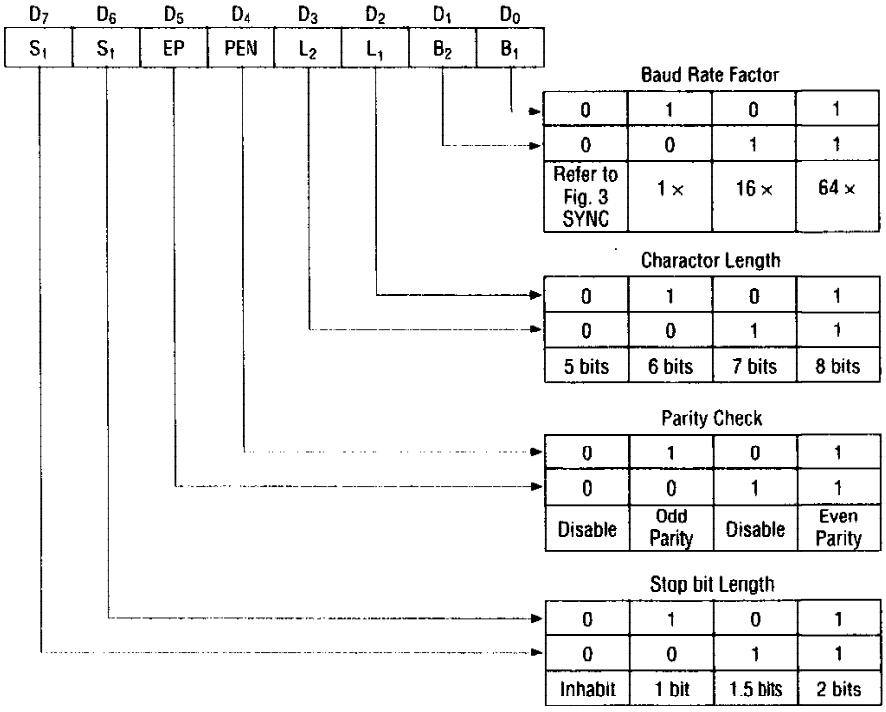


Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

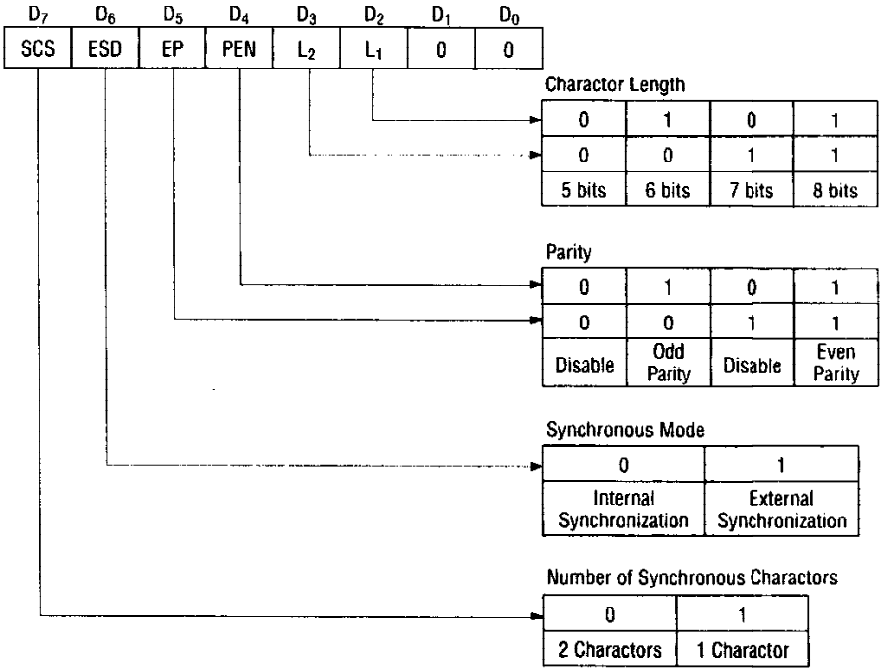


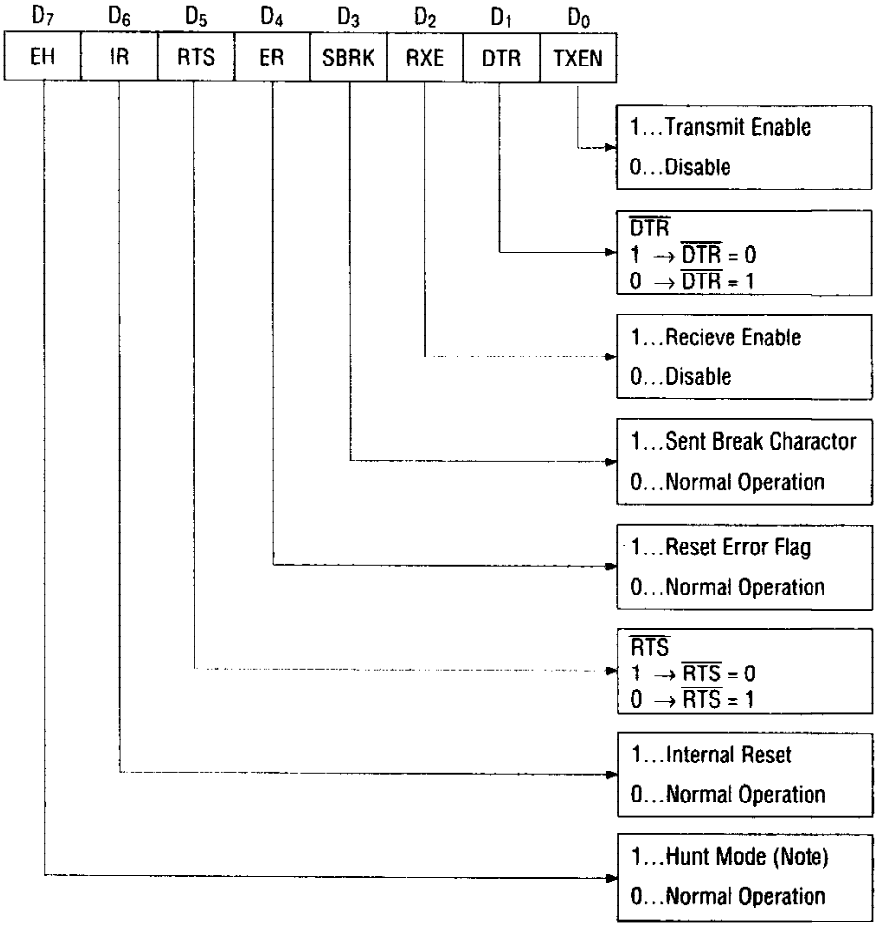
Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

2) Command

Command is used for setting the operation of the MSM82C51A-2.
It is possible to write a command whenever necessary after writing a mode instruction and sync characters.
Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.



Note: Seach mode for synchronous charactors in synchronous mode.

Fig. 4 Bit Configuration of Command

Status Word

It is possible to see the internal status of MSM82C51A-2 by reading a status word.
The bit configuration of status word is shown in Fig. 5.

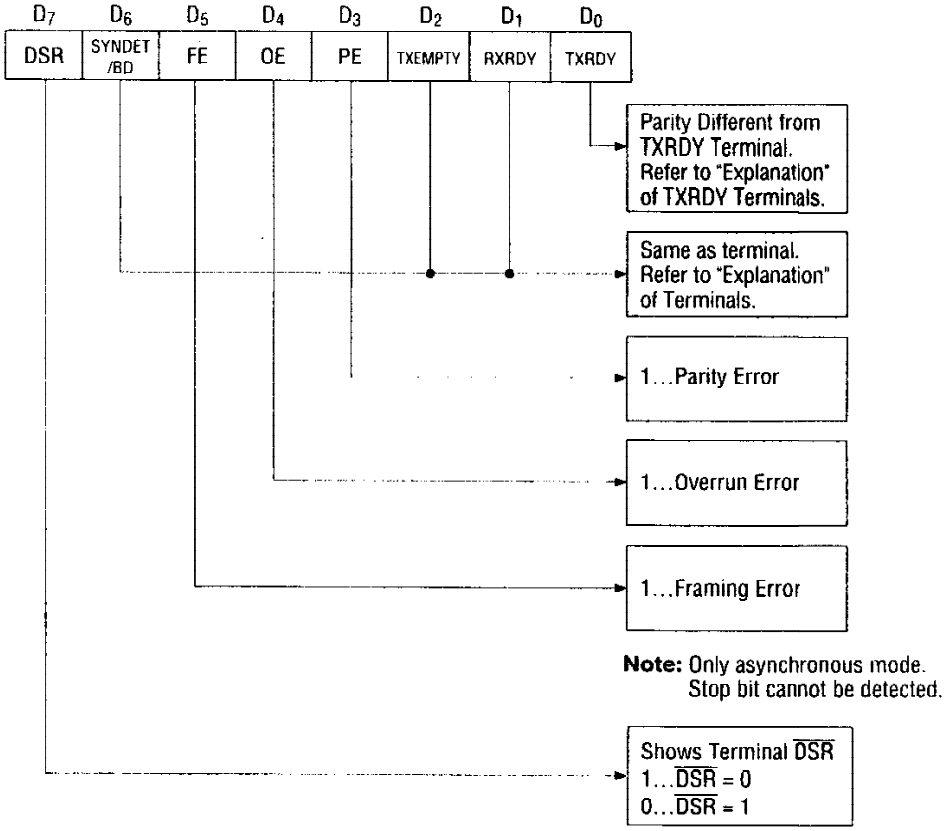


Fig. 5 Bit Configuration of Status Word

Standby Status

It is possible to put the MSM82C51A-2 in "standby status"
When the following conditions have been satisfied the MSM82C51A-2 is in "standby status."

(1) $\overline{CS}$ terminal is fixed at Vcc level.
(2) Input pins other $\overline{CS}$, D_0 to D_7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are fixed at Vcc or GND level (including SYNDET in external synchronous mode).

Note: When all output currents are 0, ICCS specification is applied.

Pin Description

D_0 to D_7 (I/O terminal)
This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)
A "High" on this input forces the MSM82C51A-2 into "reset status."
The device waits for the writing of "mode instruction."
The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)
CLK signal is used to generate internal device timing.
CLK signal is independent of $\overline{RXC}$ or $\overline{TXC}$.
However, the frequency of CLK must be greater than 30 times the $\overline{RXC}$ and $\overline{TXC}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{WR}$ (Input terminal)
This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the MSM82C51A-2.

$\overline{RD}$ (Input terminal)
This is the "active low" input terminal which receives a signal for reading receive data and status words from the MSM82C51A-2.

C/$\overline{D}$ (Input terminal)
This is an input terminal which receives a signal for selecting data or command words and status words when the MSM82C51A-2 is accessed by the CPU.
If C/$\overline{D}$ = low, data will be accessed.
If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input terminal)
This is the "active low" input terminal which selects the MSM82C51A-2 at low level when the CPU accesses.

Note: The device won't be in "standby status"; only setting $\overline{CS}$ = High.
Refer to "Explanation of Standby Status."

TXD (output terminal)
This is an output terminal for transmitting data from which serial-converted data is sent out.
The device is in "mark status" (high level) after resetting or during a status when transmit is disabled.
It is also possible to set the device in "break status" (low level) by a command.

TXRDY (output terminal)
This is an output terminal which indicates that the MSM82C51A-2 is ready to accept a transmitted data character. But the terminal is always at low level if $\overline{CTS}$ = high or the device was set in "TX disable status" by a command.

Note: TXRDY status word indicates that transmit data character is receivable, regardless of $\overline{CTS}$ or command.
If the CPU writes a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output terminal)
This is an output terminal which indicates that the MSM82C51A-2 has transmitted all the characters and had no data character.
In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

Note : As the transmitter is disabled by setting $\overline{CTS}$ "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High".
Even if a data is written after disable, that data is not sent out and TXE will be "High". After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

$\overline{TXC}$ (Input terminal)
This is a clock input signal which determines the transfer speed of transmitted data.
In "synchronous mode," the baud rate will be the same as the frequency of $\overline{TXC}$.
In "asynchronous mode", it is possible to select the baud rate factor by mode instruction.
It can be 1, 1/16 or 1/64 the $\overline{TXC}$.
The falling edge of $\overline{TXC}$ sifts the serial data out of the MSM82C51A-2.

RXD (input terminal)
This is a terminal which receives serial data.

RXRDY (Output terminal)
This is a terminal which indicates that the MSM82C51A-2 contains a character that is ready to READ.
If the CPU reads a data character, RXRDY will be reset by the leading edge of $\overline{RD}$ signal.
Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

$\overline{RXC}$ (Input terminal)
This is a clock input signal which determines the transfer speed of received data.
In "synchronous mode," the baud rate is the same as the frequency of $\overline{RXC}$.
In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.
It can be 1, 1/16, 1/64 the $\overline{RXC}$.

SYNDET/BD (Input or output terminal)
This is a terminal whose function changes according to mode.
In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset.
In "external synchronous mode, "this is an input terminal.
A "High" on this input forces the MSM82C51A-2 to start receiving data characters.
In "asynchronous mode," this is an output terminal which generates "high level"output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.
After Reset is active, the terminal will be output at low level.

$\overline{\text{DSR}}$ (Input terminal)
This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

$\overline{\text{DTR}}$ (Output terminal)
This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{DTR}}$ by a command.

$\overline{\text{CTS}}$ (Input terminal)
This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

$\overline{\text{RTS}}$ (Output terminal)
This is an output port for MODEM interface. It is possible to set the status $\overline{\text{RTS}}$ by a command.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating			Unit	Conditions
		MSM82C51A-2RS	MSM82C51A-2GS	MSM82C51A-2JS		
Power Supply Voltage	V_{CC}	−0.5 to +7			V	With respect to GND
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5			V	
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5			V	
Storage Temperature	T_{STG}	−55 to +150			°C	—
Power Dissipation	P_D	0.9	0.7	0.9	W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	3 - 6	V
Operating Temperature	T_{op}	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{op}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3	—	+0.8	V
"H" Input Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V

DC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5 V Ta = −40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
"L" Output Voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.7	—	—	V	I_{OH} = −2.5 mA
Input Leak Current	I_{LI}	−10	—	10	µA	$0 \le V_{IN} \le V_{CC}$
Output Leak Current	I_{LO}	−10	—	10	µA	$0 \le V_{OUT} \le V_{CC}$
Operating Supply Current	I_{CCO}	—	—	5	mA	Asynchronous X64 during Transmitting/ Receiving
Standby Supply Current	I_{CCS}	—	—	100	µA	All Input voltage shall be fixed at V_{CC} or GND level.

AC CHARACTERISTICS

CPU Bus Interface Part

(V_{CC} = 4.5 to 5.5 V, Ta = −40 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address Stable before $\overline{RD}$	t_{AR}	20	—	ns	Note 2
Address Hold Time for $\overline{RD}$	t_{RA}	20	—	ns	Note 2
$\overline{RD}$ Pulse Width	t_{RR}	130	—	ns	—
Data Delay from $\overline{RD}$	t_{RD}	—	100	ns	—
$\overline{RD}$ to Data Float	t_{DF}	10	75	ns	—
Recovery Time between $\overline{RD}$	t_{RVR}	6	—	t_{CY}	Note 5
Address Stable before $\overline{WR}$	t_{AW}	20	—	ns	Note 2
Address Hold Time for $\overline{WR}$	t_{WA}	20	—	ns	Note 2
$\overline{WR}$ Pulse Width	t_{WW}	100	—	ns	—
Data Set-up Time for $\overline{WR}$	t_{DW}	100	—	ns	—
Data Hold Time for $\overline{WR}$	t_{WD}	0	—	ns	—
Recovery Time between $\overline{WR}$	t_{RVW}	6	—	t_{CY}	Note 4
RESET Pulse Width	t_{RESW}	6	—	t_{CY}	—

Serial Interface Part

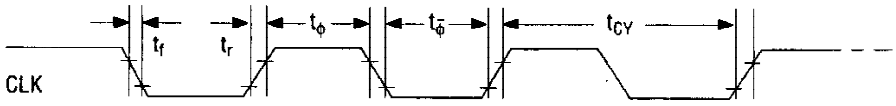
(V_{CC} = 4.5 to 5.5 V, Ta = −40 to 85°C)

Parameter		Symbol	Min.	Max.	Unit	Remarks
Main Clock Period		t_{CY}	160	—	ns	Note 3
Clock Low Tme		t_{ϕ}	50	—	ns	—
Clock High Time		t_{ϕ}	70	t_{CY} −50	ns	—
Clock Rise/Fall Time		t_r, t_f	—	20	ns	—
TXD Delay from Falling Edge of $\overline{TXC}$		t_{DTX}	—	1	µS	—
Transmitter Clock Frequency	1 × Baud	f_{TX}	DC	64	kHz	Note 3
	16 × Baud	f_{TX}	DC	615	kHz	
	64 × Baud	f_{TX}	DC	615	kHz	
Transmitter Clock Low Time	1 × Baud	t_{TPW}	13	—	t_{CY}	—
	16 ×, 64 × Baud	t_{TPW}	2	—	t_{CY}	—
Transmitter Clock High Time	1 × Baud	t_{TPD}	15	—	t_{CY}	—
	16 ×, 64 × Baud	t_{TPD}	3	—	t_{CY}	—
Receiver Clock Frequency	1 × Baud	f_{RX}	DC	64	kHz	Note 3
	16 × Baud	f_{RX}	DC	615	kHz	
	64 × Baud	f_{RX}	DC	615	kHz	
Receiver Clock Low Time	1 × Baud	t_{RPW}	13	—	t_{CY}	—
	16 ×, 64 × Baud	t_{RPW}	2	—	t_{CY}	—
Receiver Clock High Time	1 × Baud	t_{RPD}	15	—	t_{CY}	—
	16 ×, 64 × Baud	t_{RPD}	3	—	t_{CY}	—
Time from the Center of Last Bit to the Rise of TXRDY		t_{TXRDY}	—	8	t_{CY}	—
Time from the Leading Edge of $\overline{WR}$ to the Fall of TXRDY		$t_{TXRDY\ CLEAR}$	—	400	ns	—
Time From the Center of Last Bit to the Rise of RXRDY		t_{RXRDY}	—	26	t_{CY}	—
Time from the Leading Edge of $\overline{RD}$ to the Fall of RXRDY		$t_{RXRDY\ CLEAR}$	—	400	ns	—
Internal SYNDET Delay Time from Rising Edge of $\overline{RXC}$		t_{IS}	—	26	t_{CY}	—
SYNDET Setup Time for $\overline{RXC}$		t_{ES}	18	—	t_{CY}	—
TXE Delay Time from the Center of Last Bit		$t_{TXEMPTY}$	20	—	t_{CY}	—
MODEM Control Signal Delay Time from Rising Edge of $\overline{WR}$		t_{WC}	8	—	t_{CY}	—
MODEM Control Signal Setup Time for Falling Edge of $\overline{RD}$		t_{CR}	20	—	t_{CY}	—
RXD Setup Time for Rising Edge of $\overline{RXC}$ (1X Baud)		t_{RXDS}	11	—	t_{CY}	—
RXD Hold Time for Falling Edge of $\overline{RXC}$ (1X Baud)		t_{RXDH}	17	—	t_{CY}	—

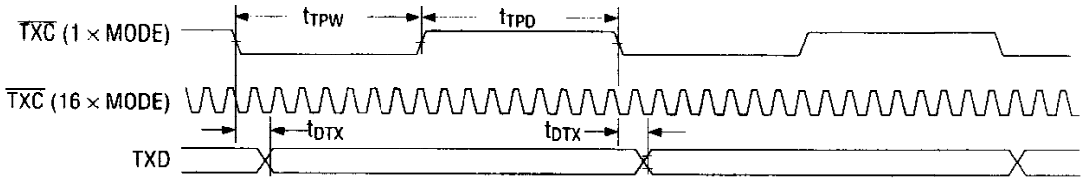
Notes:
1. AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.
2. Addresses are $\overline{CS}$ and C/$\overline{D}$.
3. f_{TX} or $f_{RX} \leq 1/(30\ Tcy)$ 1× Baud
   f_{TX} or $f_{RX} \leq 1/(5\ Tcy)$ 16×, 64× Baud
4. This recovery time is mode Initialization only. Recovery time between command writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 18 t_{CY}.
   Write Data is allowed only when TXRDY = 1.
5. This recovery time is Status read only.
   Read Data is allowed only when RXRDY = 1.
6. Status update can have a maximum delay of 28 clock periods from event affecting the status.

TIMING CHART

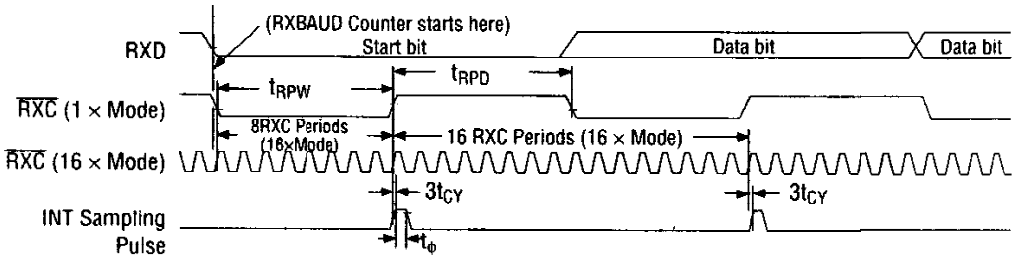
Sytem Clock Input



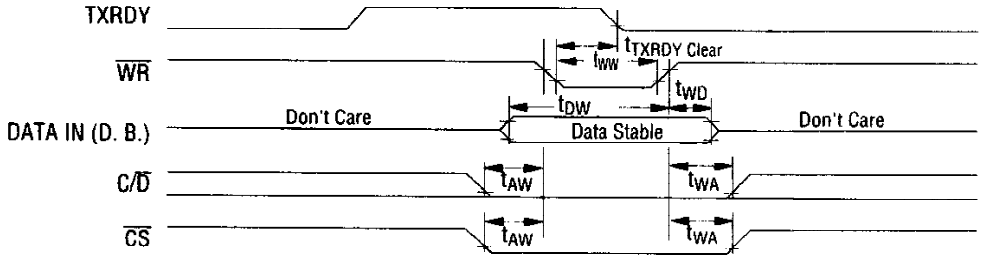
Transmitter Clock and Data



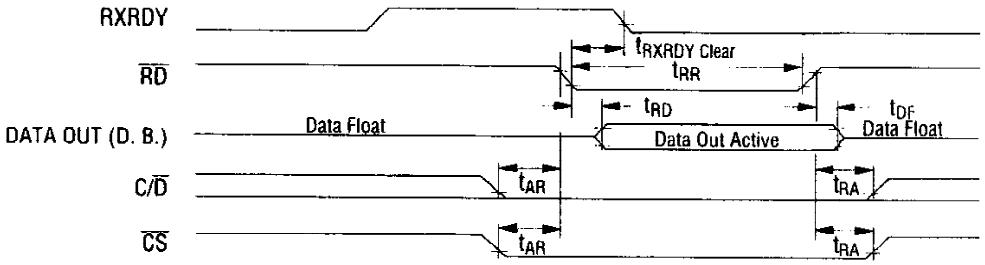
Receiver Clock and Data



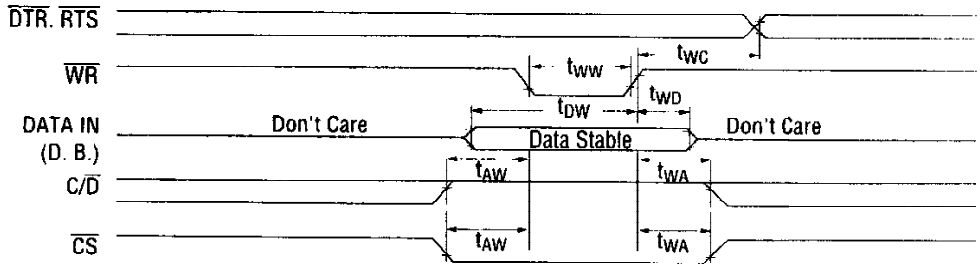
Write Data Cycle (CPU → USART)



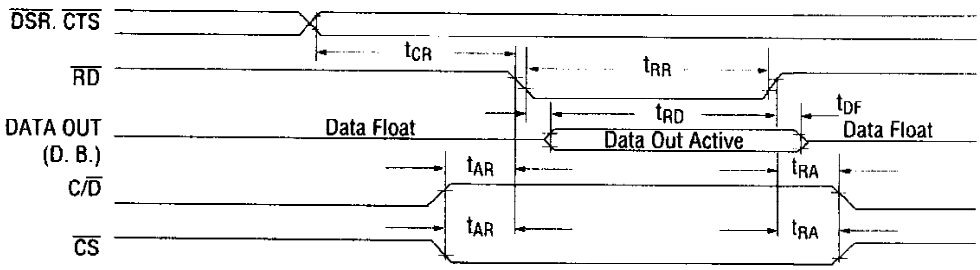
Read Data Cycle (CPU ← USART)



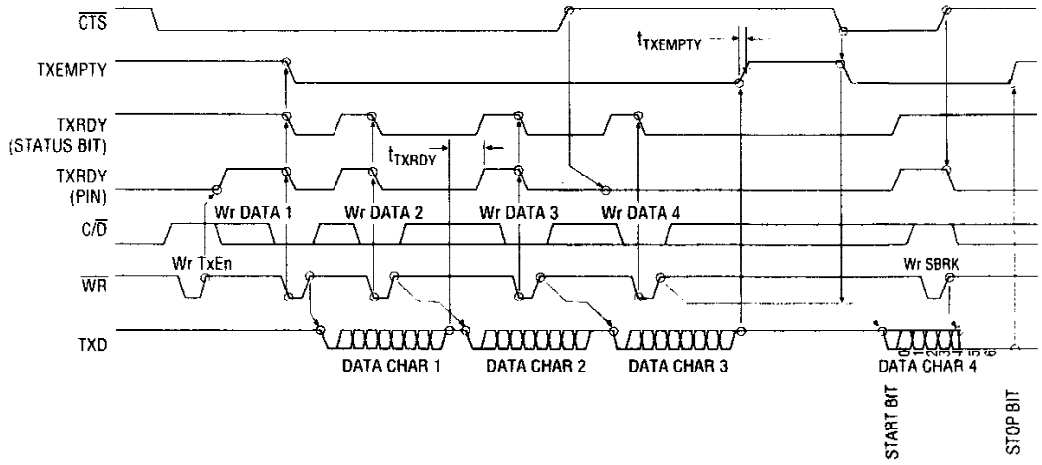
Write Control or Output Port Cycle (CPU → USART)



Read Control or Input Port Cycle (CPU ← USART)

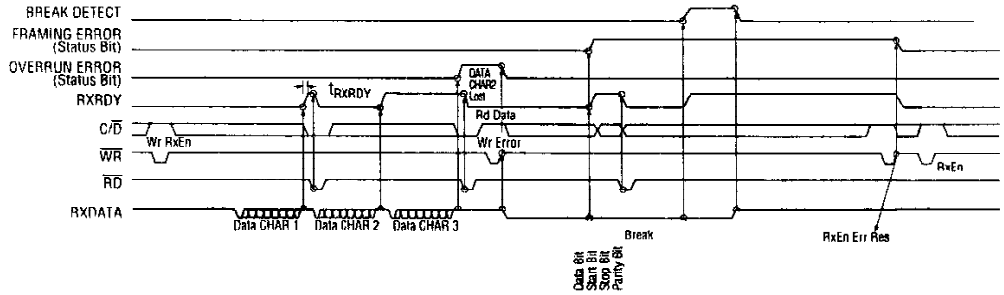


Transmitter Control and Flag Timing (ASYNC Mode)



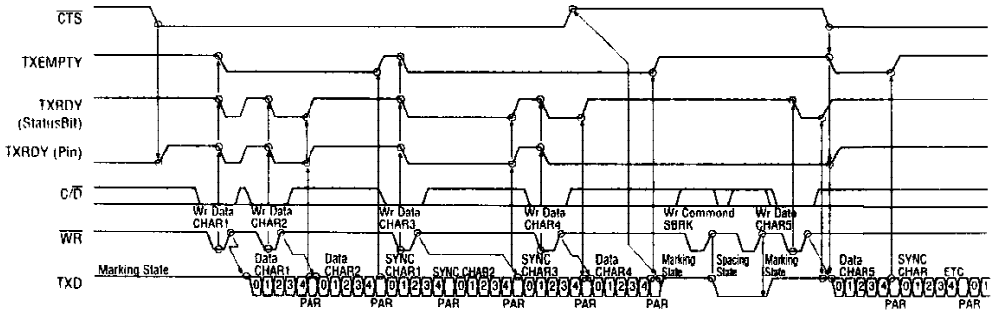
Note: The wave-form chart is based on the case of 7-bit data length + parity bit + 2 stop bit.

Receiver Control and Flag Timing (ASYNC Mode)



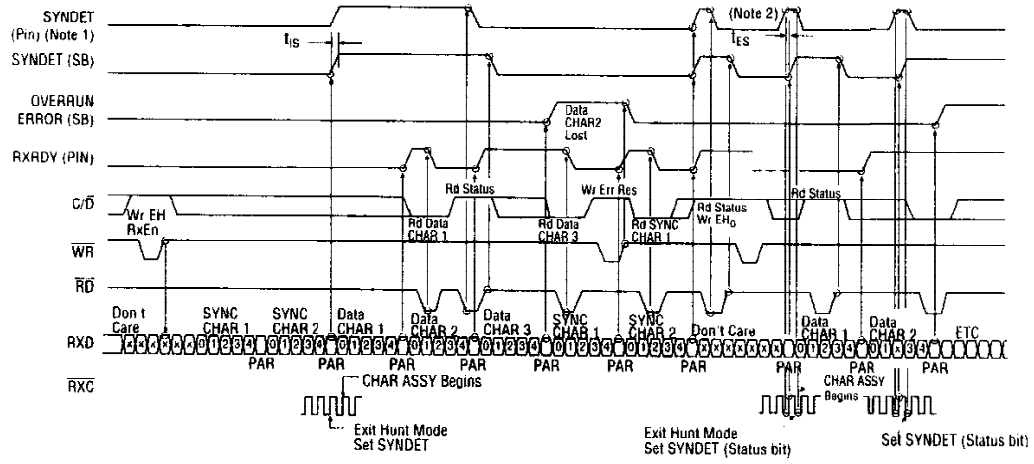
Note: The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.

Transmitter Control and Flag Timing (SYNC Mode)



Note: The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous charactors.

Receiver Control and Flag Timing (SYNC Mode)



Note: 1. Internal Synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous charactor.
2. External Synchronization is based on the case of 5 data bit length + parity bit.

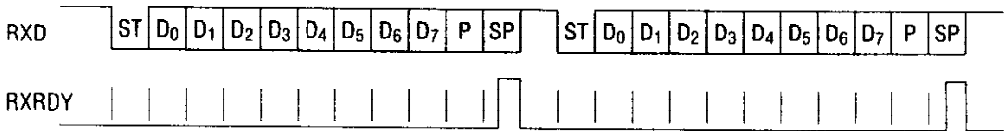
Note: 1. Half-bit processing for the start bit
When the MSM82C51A-2 is used in the asynchronous mode, some problems are caused in the processing for the start bit whose length is smaller than the 1-data bit length. (See Fig. 1.)

Start bit Length	Mode	Operation
Smaller than 7-Receiver Clock Length	×16	The short start bit is ignored. (Normal)
Smaller than 31-Receiver Clock Length	×64	The short start bit is ignored. (Normal)
8-Receiver Clock Length	×16	Data cannot be received correctly due to a malfunction.
32-Receiver Clock Length	×64	Data cannot be received correctly due to a malfunction.
9 to 16-Receiver Clock Length	×16	The bit is regarded as a start bit. (normal)
33 to 64-Receiver Clock Length	×64	The bit is regarded as a start bit. (normal)

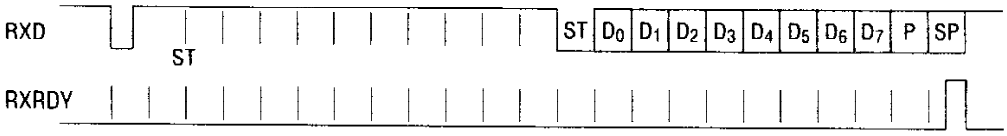
2. Parity flag after a break signal is received (See Fig. 2.)
When the MSM82C51A-2 is used in the asynchrous mode, a parity flag may be set when the next normal data is read after a break signal is received. (This occurs when odd parity is set.)
A parity flag is set when the rising edge of the break signal (end of the break signal) is changed between the final data bit and the parity bit, through a RXRDY signal may not be outputted.
If this occurs, the parity flag is left set when the next normal dats is received, and the received data seems to be a parity error.

Half-bit Processing Timing Chart for the Start bit (Fig. 1)

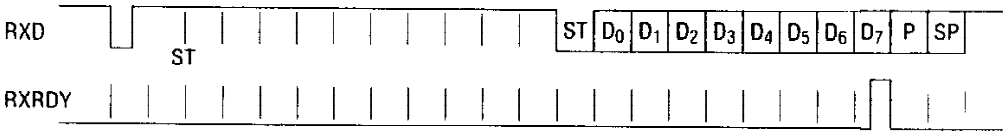
Normal Operation



The Start bit Is Shorter Than a 1/2 Data bit

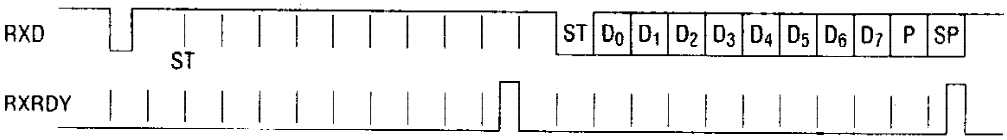


The Start bit Is a 1/2 Data bit (A problem of MSM82C51A-2)



A RXRDY signal is outputted during data reception due to a malfunction.

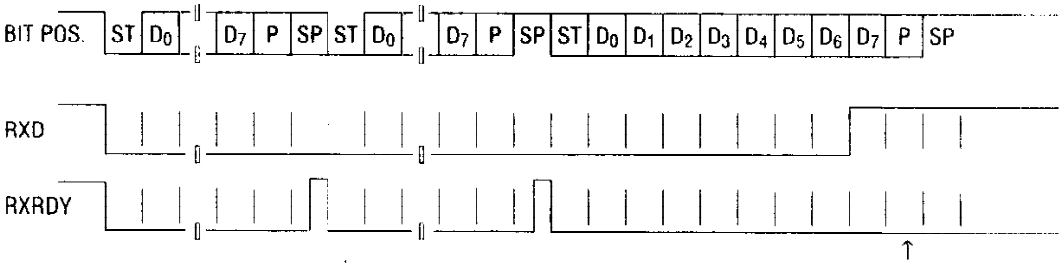
The Start bit Is Longer Than a 1/2 Data bit



ST: Start bit
SP: Stop bit
P: Parity bit
D_0 - D_7: Data bits

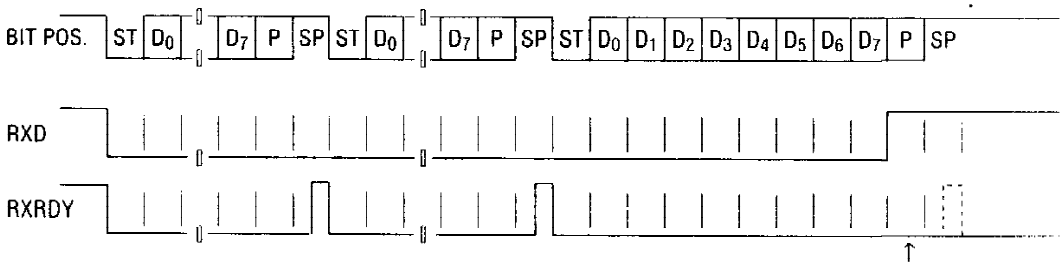
Break Signal Reception Timing and Parity Flag (Fig. 2)

Normal Operation



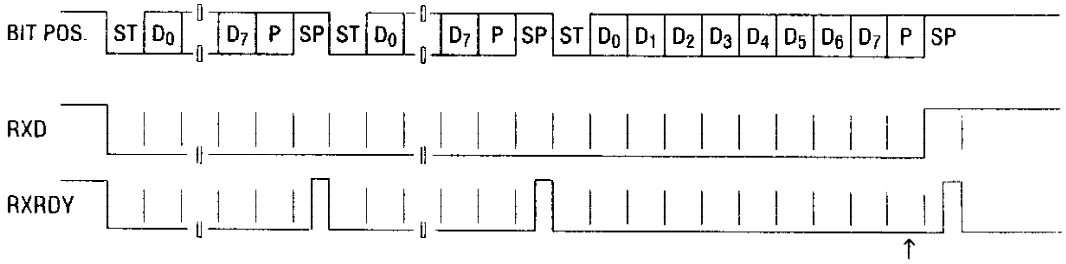
No parity flag is set. and no RXRDY signal is outputted.

Bug Timing



A parity flag is set, but, no RXRDYsignal is outputted.

Normal Operation



A parity flag is set. and a RXRDY signal is outputted.