General Information 1

TTL Devices 2

Mechanical Data 3

Contents

Title	Page
NUMERICAL INDEX	1-3
FUNCTIONAL INDEX	1-7
GLOSSARY	1-39
EXPLANATION OF FUNCTION TABLES	1-43
PARAMETER MEASUREMENT INFORMATION	1-45
TYPICAL CHARACTERISTICS	1-51

Device Type		Page No.	Device Type		Page No.
SN5400	SN7400	2-3	SN54S30	SN74S30	2-127
SN54LS00	SN74LS00	2-3	SN54LS31	SN74LS31	2-133
SN54S00	SN74S00	2-3	SN5432	SN7432	2-137
SN5401	SN7401	2-9	SN54LS32	SN74LS32	2-137
SN54LS01	SN74LS01	2-9	SN54S32	SN74S32	2-137
SN5402	**SN7402**	**2-13**	**SN5433**	**SN7433**	**2-143**
SN54LS02	**SN74LS02**	**2-13**	**SN54LS33**	**SN74LS33**	**2-143**
SN54S02	SN74S02	2-13	SN5437	SN7437	2-147
SN5403	SN7403	2-19	SN54LS37	SN74LS37	2-147
SN54LS03	SN74LS03	2-19	SN54S37	SN74S37	2-147
SN54S03	SN74S03	2-19	SN5438	SN7438	2-153
SN5404	SN7404	2-25	SN54LS38	SN74LS38	2-153
SN54LS04	SN74LS04	2-25	SN54S38	SN74S38	2-153
SN54S04	SN74S04	2-25	SN5439	SN7439	2-159
SN5405	SN7405	2-31	SN5440	SN7440	2-161
SN54LS05	SN74LS05	2-31	SN54LS40	SN74LS40	2-161
SN54S05	SN74S05	2-31	SN54S40	SN74S40	2-161
SN5406	SN7406	2-37	SN5442A	SN7442A	2-167
SN5407	SN7407	2-39	SN54LS42	SN74LS42	2-167
SN5408	SN7408	2-41	SN5445	SN7445	2-173
SN54LS08	SN74LS08	2-41	SN5446A	SN7446A	2-175
SN54S08	SN74S08	2-41	SN5447A	SN7447A	2-175
SN5409	SN7409	2-47	SN54LS47	SN74LS47	2-175
SN54LS09	SN74LS09	2-47	SN5448	SN7448	2-175
SN54S09	SN74S09	2-47	SN54LS48	SN74LS48	2-175
SN5410	SN7410	2-53	SN54LS49	SN74LS49	2-175
SN54LS10	SN74LS10	2-53	SN5450	SN7450	2-189
SN54S10	SN74S10	2-53	SN5451	SN7451	2-193
SN54LS11	SN74LS11	2-59	SN54LS51	SN74LS51	2-193
SN54S11	SN74S11	2-59	SN54S51	SN74S51	2-193
SN5412	SN7412	2-63	SN5453	SN7453	2-199
SN54LS12	SN74LS12	2-63	SN5454	SN7454	2-201
SN5413	SN7413	2-67	SN54LS54	SN74LS54	2-201
SN54LS13	SN74LS13	2-67	SN54LS55	SN74LS55	2-205
SN5414	SN7414	2-77	SN54LS56	SN74LS56	2-207
SN54LS14	SN74LS14	2-77	SN54LS57	SN74LS57	2-207
SN54LS15	SN74LS15	2-87	SN54S64	SN74S64	2-211
SN54S15	SN74S15	2-87	SN54S65	SN74S65	2-211
SN5416	SN7416	2-37	SN54LS68	SN74LS68	2-215
SN5417	SN7417	2-39	SN54LS69	SN74LS69	2-215
	SN74LS19A	2-91	SN5470	SN7470	2-221
SN5420	SN7420	2-95	SN5472	SN7472	2-225
SN54LS20	SN74LS20	2-95	SN5473	SN7473	2-229
SN54S20	SN74S20	2-95	SN54LS73A	SN74LS73A	2-229
SN54LS21	SN74LS21	2-101	SN5474	SN7474	2-235
SN5422	SN7422	2-105	SN54LS74A	SN74LS74A	2-235
SN54LS22	SN74LS22	2-105	SN54S74	SN74S74	2-235
SN54S22	SN74S22	2-105	SN5475	SN7475	2-241
SN5423	SN7423	2-111	SN54LS75	SN74LS75	2-241
	SN74LS24A	2-91	SN5476	SN7476	2-247
SN5425	SN7425	2-111	SN54LS76A	SN74LS76A	2-247
SN5426	SN7426	2-115	SN5477		2-241
SN54LS26	SN74LS26	2-115	SN54LS77		2-241
SN5427	SN7427	2-119	SN54LS78A	SN74LS78A	2-253
SN54LS27	SN74LS27	2-119	SN5483A	SN7483A	2-257
SN5428	SN7528	2-123	SN54LS83A	SN74LS83A	2-257
SN54LS28	SN74LS28	2-123	SN5485	SN7485	2-263
SN5430	SN7430	2-127	SN54LS85	SN74LS85	2-263
SN54LS30	SN74LS30	2-127	SN54S85	SN74S85	2-263

Device Type		Page No.	Device Type		Page No.
SN5486	SN7486	2-271	SN54143	SN74143	2-439
SN54LS86A	SN74LS86A	2 271	SN54145	SN74145	2-447
SN54S86	SN74S86	2-271	SN54LS145	SN74LS145	2-447
SN5490A	SN7490A	2-277	SN54147	SN74147	2-451
SN54LS90	SN74LS90	2-277	SN54LS147	SN74LS147	2-451
SN5491A	SN7491A	2-289	SN54148	SN74148	2-451
SN54LS91	SN74LS91	2 289	SN54LS148	SN74LS148	2-451
SN5492A	SN7492A	2 277	SN54150	SN74150	2-457
SN54LS92	SN74LS92	2 277	SN54151A	SN74151A	2-457
SN5493A	SN7493A	2-277	SN54LS151	SN74LS151	2-457
SN54LS93	SN74LS93	2-277	SN54S151	SN74S151	2 457
SN5494	SN7494	2-293	SN54153	SN74153	2-465
SN5495A	SN7495A	2-297	SN54LS153	SN74LS153	2-465
SN54LS95B	SN74LS95B	2 297	SN54S153	SN74S153	2 465
SN5496	SN7496	2-305	SN54154	SN74154	2 471
SN54LS96	SN74LS96	2 305	SN54155	SN74155	2-475
SN5497	SN7497	2 311	SN54LS155A	SN74LS155A	2-475
SN54107	**SN74107**	**2-319**	**SN54156**	**SN74156**	**2-475**
SN54LS107A	**SN74LS107A**	**2-319**	**SN54LS156**	**SN74LS156**	**2-475**
SN54109	SN74109	2 325	SN54157	SN74157	2-483
SN54LS109A	SN74LS109A	2-325	SN54LS157	SN74LS157	2-483
SN54111	SN74111	2-331	SN54S157	SN74S157	2-483
SN54LS112A	SN74LS112A	2-335	SN54LS158	SN74LS158	2 483
SN54S112	SN74S112	2-335	SN54S158	SN74S158	2-483
SN54LS113A	SN74LS113A	2-343	SN54159	SN74159	2-489
SN54S113	SN74S113	2-343	SN54160	SN74160	2-493
SN54LS114A	SN74LS114A	2-349	SN54LS160A	SN74LS160A	2-493
SN54S114	SN74S114	2-349	SN54161	SN74161	2-493
SN54116	SN74116	2-357	SN54LS161A	SN74LS161A	2-493
SN54120	SN74120	2-361	SN54162	SN74162	2 493
SN54121	SN74121	2 367	SN54LS162A	SN74LS162A	2-493
SN54122	SN74122	2-373	SN54S162	SN74S162	2-493
SN54LS122	SN74LS122	2-373	SN54163	SN74163	2-493
SN54123	SN74123	2 373	SN54LS163A	SN74LS163A	2-493
SN54LS123	SN74LS123	2-373	SN54S163	SN74S163	2-493
SN54S124	SN74S124	2 383	SN54164	SN74164	2-515
SN54125	SN74125	2 387	SN54LS164	SN74LS164	2-515
SN54LS125A	SN74LS125A	2-387	SN54165	SN74165	2-521
SN54126	SN74126	2 387	SN54LS165A	SN74LS165A	2-521
SN54LS126A	SN74LS126A	2-387	SN54166	SN74166	2-529
SN54128	SN74128	2-393	SN54LS166A	SN74LS166A	2 529
SN54130	SN74130	2-373	SN54167	SN74167	2-537
SN54132	SN74132	2-395	SN54LS169B	SN74LS169B	2-543
SN54LS132	SN74LS132	2 395	SN54S169	SN74S169	2-543
SN54S132	SN74S132	2 395	SN54170	SN74170	2-555
SN54S133	SN74S133	2 407	SN54LS170	SN74LS170	2-555
SN54S134	SN74S134	2-411	SN54LS171	SN74LS171	2-565
SN54S135	SN74S135	2-415		SN74172	2-569
SN54136	SN74136	2-417	SN54173	SN74173	2-575
SN54LS136	SN74LS136	2-417	SN54LS173A	SN74LS173A	2-575
SN54LS137	SN74LS137	2 421	SN54174	SN74174	2-581
SN54LS138	SN74LS138	2-425	SN54LS174	SN74LS174	2-581
SN54S138	SN74S138A	2-425	SN54S174	SN74S174	2-581
SN54LS139A	SN74LS139A	2-431	SN54175	SN74175	2-581
SN54S139	SN74S139A	2-431	SN54LS175	SN74LS175	2-581
SN54S140	SN74S140	2-435	SN54S175	SN74S175	2-581

Device Type		Page No.	Device Type		Page No.
SN54176	SN74176	2-587	SN54LS266	SN74LS266	2-757
SN54177	SN74177	2 587	SN54273	SN74273	2-759
SN54178	SN74178	2-593	SN54LS273	SN74LS273	2-759
SN54180	SN74180	2-597	SN54276	SN74276	2-763
SN54LS181	SN74LS181	2-601	SN54278	SN74278	2 767
SN54S181	**SN74S181**	**2-601**	**SN54279**	**SN74279**	**2-771**
SN54S182	**SN74S182**	**2-611**	**SN54LS279A**	**SN74LS279A**	**2-771**
SN54LS183	**SN74LS183**	**2-617**	**SN54LS280**	**SN74LS280**	**2-775**
SN54190	SN74190	2-619	SN54S280	SN74S280	2-775
SN54LS190	SN74LS190	2-619	SN54283	SN74283	2 781
SN54191	SN74191	2-619	SN54LS283	SN74LS283	2-781
SN54LS191	SN74LS191	2-619	SN54S283	SN74S283	2-781
SN54192	SN74192	2-633	SN54284	SN74284	2-787
SN54LS192	SN74LS192	2-633	SN54285	SN74285	2-787
SN54193	SN74193	2-633	SN54290	SN74290	2 791
SN54LS193	SN74LS193	2-633	SN54LS290	SN74LS290	2-791
SN54194	SN74194	2-645	SN54LS292	SN74LS292	2 799
SN54LS194A	SN74LS194A	2-645	SN54293	SN74293	2-791
SN54S194	SN74S194	2-645	SN54LS293	SN74LS293	2-791
SN54195	SN74195	2-655	SN54LS294	SN74LS294	2-799
SN54LS195A	SN74LS195A	2-655	SN54LS295B	SN74LS295B	2-807
SN54S195	SN74S195	2-663	SN54LS297	SN74LS297	2-811
SN54196	SN74196	2-663	SN54298	SN74298	2-817
SN54LS196	SN74LS196	2-663	SN54LS298	SN74LS298	2-817
SN54S196	SN74S196	2-663	SN54LS299	SN74LS299	2-823
SN54197	SN74197	2-663	SN54S299	SN74S299	2-823
SN54LS197	SN74LS197	2-663	SN54LS320	SN74LS320	2-829
SN54S197	SN74S197	2-663	SN54LS321	SN74LS321	2 829
SN54198	**SN74198**	**2-671**	**SN54LS322A**	**SN74LS322A**	**2-835**
SN54199	**SN74199**	**2-671**	**SN54ALS323**	**SN74ALS323**	**2-841**
SN54221	SN74221	2-681	SN54LS348	SN74LS348	2-845
SN54LS221	SN74LS221	2-681	SN54S350	SN74S350	2-849
SN54LS240	SN74LS240	2-691	SN54LS352	SN74LS352	2-855
SN54S240	SN74S240	2-691	SN54LS353	SN74LS353	2-859
SN54LS241	SN74LS241	2-691	SN54LS354	SN74LS354	2-863
SN54S241	SN74S241	2-691	SN54LS355	SN74LS355	2-863
SN54LS242	SN74LS242	2-697	SN54LS356	SN74LS356	2-863
SN54LS243	SN74LS243	2-697	SN54365A	SN74365A	2-873
SN54LS244	SN74LS244	2-691	SN54LS365A	SN74LS365A	2-873
SN54S244	SN74S244	2-691	SN54366A	SN74366A	2-873
SN54LS245	SN74LS245	2-701	SN54LS366A	SN74LS366A	2-873
SN54246	SN74246	2-705	SN54367A	SN74367A	2-873
SN54247	SN74247	2-705	SN54LS367A	SN74LS367A	2 873
SN54LS247	SN74LS247	2-705	SN54368A	SN74368A	2-873
SN54LS248	SN74LS248	2-705	SN54LS368A	SN74LS368A	2-873
SN54251	SN74251	2-715	SN54LS373	SN74LS373	2-883
SN54LS251	SN74LS251	2-715	SN54S373	SN74S373	2-883
SN54S251	SN74S251	2-715	SN54LS374	SN74LS374	2-883
SN54LS253	SN74LS253	2-723	SN54S374	SN74S374	2-883
SN54S253	SN74S253	2-723	SN54LS375	SN74LS375	2 891
SN54LS257B	SN74LS257B	2 729	SN54376	SN74376	2 893
SN54S257	SN74S257	2-729	SN54LS377	SN74LS377	2-895
SN54LS258B	SN74LS258B	2-729	SN54LS378	SN74LS378	2-895
SN54S258	SN74S258	2-729	SN54LS379	SN74LS379	2-895
SN54259	SN74259	2-735	SN54LS381A	SN74LS381A	2-899
SN54LS259B	SN74LS259B	2-735	SN54S381	SN74S381	2-899
SN54S260	SN74S260	2-739	SN54LS382	SN74LS382	2 899
SN54LS261	SN74LS261	2-743	SN54LS384	SN74LS384	2 907
SN54265	SN74265	2-751	SN54LS385	SN74LS385	2-913

Device Type		Page No.	Device Type		Page No.
SN54LS386A	SN74LS386A	2-917	SN54LS621	SN74LS621	2-1031
SN54390	SN74390	2-919		SN74LS623	2-1031
SN54LS390	SN74LS390	2-919	SN54LS624	SN74LS624	2-1037
SN54393	SN74393	2-919		SN74LS625	2-1037
SN54LS393	SN74LS393	2-919	SN54LS626	SN74LS626	2-1037
SN54LS395A	SN74LS395A	2-929		SN74LS627	2-1037
SN54LS396	SN74LS396	2-933	SN54LS628	SN74LS628	2-1037
SN54LS399	SN74LS399	2-937	SN54LS629	SN74LS629	2-1037
SN54LS422	SN74LS422	2-941	SN54LS630	SN74LS630	2-1047
SN54LS423	SN74LS423	2-941	SN54LS636	SN74LS636	2-1055
SN54S436	SN74S436	2-947	SN54LS637	SN74LS637	2-1055
SN54LS440	SN74LS440	2-951	SN54LS638	SN74LS638	2-1063
SN54LS441	SN74LS441	2-951	SN54LS639	SN74LS639	2-1063
SN54LS442	SN74LS442	2-951	SN54LS640	SN74LS640	2-1067
SN54LS444	SN74LS444	2-951	SN54LS641	SN74LS641	2-1067
SN54LS445	SN74LS445	2-957	SN54LS642	SN74LS642	2-1067
SN54LS446	SN74LS446	2-959	SN54LS644	SN74LS644	2-1067
SN54LS449	SN74LS449	2-959	SN54LS645	SN74LS645	2-1067
SN54LS465	SN74LS465	2-963	SN54LS646	SN74LS646	2-1075
SN54LS466	SN74LS466	2-963	SN54LS647	SN74LS647	2-1075
SN54LS467	SN74LS467	2-963	SN54LS648	SN74LS648	2-1075
SN54LS468	SN74LS468	2-963	SN54LS649	SN74LS649	2-1075
SN54LS490	SN74LS490	2-967	SN54LS651	SN74LS651	2-1085
SN54LS540	SN74LS540	2-973	SN54LS652	SN74LS652	2-1085
SN54LS541	SN74LS541	2-973	SN54LS653	SN74LS653	2-1085
SN54LS590	SN74LS590	2-977	SN54LS668	SN74LS668	2-1093
SN54LS591	SN74LS591	2-977	SN54LS669	SN74LS669	2-1093
SN54LS592	SN74LS592	2-981	SN54LS670	SN74LS670	2-1103
SN54LS593	SN74LS593	2-981	SN54LS671	SN74LS671	2-1111
SN54LS594	SN74LS594	2-989	SN54LS672	SN74LS672	2-1111
SN54LS595	SN74LS595	2-993	SN54LS673	SN74LS673	2-1117
SN54LS596	SN74LS596	2-993	SN54LS674	SN74LS674	2-1117
SN54LS597	SN74LS597	2-999	SN54LS681	SN74LS681	2-1123
SN54LS598	SN74LS598	2-999	SN54LS682	SN74LS682	2-1129
SN54LS599	SN74LS599	2-989	SN54LS684	SN74LS684	2-1129
	SN74LS600A	2-1007	SN54LS685	SN74LS685	2-1129
	SN74LS601A	2-1007		SN74LS686	2-1129
	SN74LS603A	2-1007	SN54LS687	SN74LS687	2-1129
SN54LS604	SN74LS604	2-1015	SN54LS688	SN74LS688	2-1129
SN54LS606	SN74LS606	2-1015	SN54LS690	SN74LS690	2-1139
SN54LS607	SN74LS607	2-1015	SN54LS691	SN74LS691	2-1139
SN54LS610	SN74LS610	2-1021	SN54LS693	SN74LS693	2-1139
	SN74LS611	2-1021	SN54LS696	SN74LS696	2-1149
SN54LS612	SN74LS612	2-1021	SN54LS697	SN74LS697	2-1149
	SN74LS613	2-1021	SN54LS699	SN74LS699	2-1149
SN54LS620	SN74LS620	2-1031			

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Column heading Literature Number provides the latest available technical source for a particular product. TI's technical literature is identified by a seven- or eight-character product source code consisting of four (4) alpha characters, three (3) numeric characters, and a revision letter, if applicable. If the fourth alpha character is an "S", then the document is a stand-alone data sheet, e.g., SDAS106A. The code is printed at the upper right-hand corner on the front cover and the lower left-hand corner on the back cover of a data book, and at the lower left-hand corner on the back page of a data sheet.

List of Applicable Databooks:

SCAD001A = Advanced CMOS Logic Databook
SCLD001B = High-Speed CMOS Logic Databook
SDAD001B = ALS/AS Logic Databook
SDFD001 = F Logic Databook
SDLD001A = Standard TTL Logic Databook
SDVD001 = LSI Logic Databook
SDZD001B = Programmable Logic Databook

GATES

POSITIVE-NAND GATES

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
8-Input	'30	●	●	●							SDLD001A
					A	●					[illegible]
								●			SC[illegible]
							●				SD[illegible]
	'11030								●	●	SC[illegible]
13-Input	'133				●						SD[illegible]
								●			SC[illegible]
				●							[illegible]
12-Input	'134			●							[illegible]
Dual 2-Input	'8003				●						SDAD001B
Dual 4-Input	'13	●	●								SDLD001A
	'20	●	●	●							SDL[illegible]
					A	●					SD[illegible]
								●			[illegible]
							●				[illegible]
	'40				A						[illegible]0001B
		●	●	●							0001A
	'1020				A						SD[illegible]
	'11020								●	●	SC[illegible]
Triple 3-Input	'10	●	●	●							SDLD001A
					●	●					SDAD001B
								●			[illegible]0001B
							●				[illegible]0001
	'1010				A						SD[illegible]
	'11010								●	●	SC[illegible]
Quad 2-Input	'00				A	●					SDAD001B
		●	●	●							SD[illegible]
								●			SC[illegible]
							●				SDL[illegible]
	'26	●	●								SDL[illegible]
	'37	●	●	●							SDL[illegible]
					A						SD[illegible]
	'38	●	●	●							SDL[illegible]
					A						SDAD001B
	'39	●									SDLD001A
	'132	●	●	●							[illegible]0001A
								●			[illegible]0001B
	'[illegible]				A	A					[illegible]0001B
	'1[illegible]								●	●	[illegible]0001A
Hex 2-Input	'804				A	B					SDAD001B
								●			SC[illegible]
	'1804				A	●					SD[illegible]

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
Dual 4-Input	'22	●		●							SDLD001A
					B						SDAD001B
Triple 3-Input	'12	●	●								SDLD001A
					A						SDAD001B
Quad 2-Input	'01	●	●								SDLD001A
					●						SDAD001B
								●			)001B
	'03	●	●	●							)001A
					B						D001B
								●			)001B
	'1003				A						SDAD001B

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
Triple 3-Input	'15		●	●							SDLD001A
					A						SDAD001B
Quad 2-Input	'09	●	●	●							SDLD001A
					●						SDAD001B
								●			SCLD001B
							●				SDFD001
Quad Schmitt	'7001							●			SCLD001B

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
Dual 4-Input	'21				A	●					SDAD001B
			●								SD A
								●			SC B
							●				SD
	'11021								●	●	SC A
Triple 3-Input	'11		●	●							SDL A
					A	●					SDA B
								●			B
							●				
	'1011				A						SDAD001B
	'11011								●	●	SCAD A
Quad 2-Input	'08	●	●	●							A
					●	●					SDAD001B
								●			SCLD001B
							●				SDFD001
	'1008				A	A					SDAD001B
	'11008								●	●	SCAD001A

POSITIVE-OR GATES

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
Triple 3-Input	'4075							●			SCLD001B
Quad 2-Input	'32	●	●	●							SDLD001A
					●	●					SDAD001B
								●			B
							●				
					A	A					SDAD001B
								●			001B
	'11032								●	●	SCAD001A
Hex 2-Input	'832				A	B					SDAD001B
								●			SCLD001B
	'1832				A	●					SDAD001B

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

POSITIVE-NAND GATES

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
Dual 4-Input with Strobe	'25	●									SDLD001A
Dual 4-Input	'4002							●			SCLD001B
Dual 5-Input	'260			●							SDLD001A
Triple 3-Input	'27	●	●								SDLD001A
					●	●					SDAD001B
								●			SCLD [illegible]
							●				SDFD [illegible]
	'11027								●	●	SCAD001A
Quad 2-Input	'02	●	●	●							SDLD001A
					●	●					[illegible] B
								●			[illegible] B
							●				[illegible]0001
	'28	●	●								[illegible]0001A
					A						SDAD001B
	'33	●	●								SDLD001A
					A						SDAD001B
	'36							●			SCLD001B
							●				SDFD001
	'1002				A						SDAD001B
	[illegible]					A					SDAD001B
	'7002							●			SC [illegible] B
	'11002								●	●	SC [illegible] A
Hex 2-Input	'805				A	B					[illegible] B
								●			[illegible] B
	'1805				A	●					SDAD001B

POSITIVE-OR/NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	
8-Input	'4078							A			SCLD001B

● ≡ Denotes available technology.
▲ ≡ Denotes planned new
A ≡ Denotes "A" suffix available in the technology indicated
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

EXCLUSIVE-OR/-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●	A	●				SDLD001A
					●			
							●	
							●	SCLD001B
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136	●	●					SDLD001A
					●			
						▲		SDAD001B
Quad 2-Input Exclusive-NOR Gates	'266		●					SDLD001A
							●	
	'810				●	▲		
	'7266						●	SCLD001B
Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs	'811				●	▲		SDAD001B
Quad Exclusive-OR/-NOR Gates	'135			●				SDLD001A

AND-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
2-Wide 4-Input	'55		●						SDLD001A
4-Wide 4-2-3-2 Input	'64			●					
4-Wide 2-2-3-2 Input	'54	●	●						
Dual 2-Wide 2-Input	'51	●	●	●					
							●		SCLD001B

AND-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
4-Wide 4-2-3-2-Input	'65			●					SDLD001A

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Dual 2-Wide AND-OR-Invert	'50	●							SDLD001A
Dual 4-Input Positive-NOR with Strobe	'23	●							

MULTIFUNCTION GATES AND ELEMENTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Inverter,3-/4-Input NAND/NOR Combination	'7006						●		SCLD001B
6-Section NAND Invert, NOR	'7008						●		SCLD001B
Quadruple Complimentary Output Logic Element	'265	●							SDLD001A

DELAY ELEMENTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Inverting and Noninverting Elements 2-Input NAND-Buffer	'31		●						SDLD001A

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

INVERTERS/NONINVERTING BUFFERS

HEX INVERTERS/NONINVERTERS

DESCRIPTION	TYPE	TECHNOLOGY										LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	AC	ACT	HCU	
Hex Inverters	'04	●	●	●								A
					B	●						B
								●				B
											●	B
							●					SDFD001
	'11004								●	●		SCAD001A
	'05	●	●	●								SDLD001A
					A							B
								●				B
	'06	●										A
	'14	●	●									A
								●				B
	'16	●										SDLD001A
	'19		●									SDLD001A
	'1004				●	A						SDAD001B
	'1005				●							SDAD001B
Hex Noninverter	'34				●	●						SDAD001B
	'11034								●	●		SCAD001A

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

DRIVER AND BUS TRANSCEIVERS

HEX DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Hex 2-Input Driver	'808				A	B			)001B
							●		)001B
	'1808				A	●			SDAD001B
Hex Driver	'07	●							SDLD001A
	'17	●							
	'35				A				SDAD001B
	[illegible]				●	A			SDAD001B
	[illegible]				●				SDAD001B
Noninverting Hex Buffers/ Drivers	'365	A	A						)001A
							●		)001B
	'366	A	A						SDLD001A
							●		SCLD001B
	'367	A	A						SDLD001A
							●		SCLD001B
	'368	A	A						SDLD001A
							●		SCLD001B

DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Noninverting Octal Buffers, Drivers	'757					●			SDAD001B
	'760					●			
					▲				
Inverting Octal Buffers, Drivers	'756				●	●			SDAD001B
	'763				●	●			SDAD001B
Inverting and Noninverting Octal Buffers, Drivers	'762					●			SDAD001B

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	
Noninverting Quad Transceivers	'759					●			SDAD001B
Inverting Quad Transceivers	'758				●	●			SDAD001B
12-mA/24-mA/ 40-mA Sink Transceivers	'615				●				SDAD001B
	'621				A	●			SDAD001B
			●						)001A
							●		)001
	'639				A	●			SDAD001B
			●						
	'641				A	●			
			●						A
12-mA/24-mA/ 48-mA Sink Inverting Output Transceivers	'614				●				1B
	'622				A	●			B
							●		
	'638				A	●			B
			●						SLDL001A
	'642				A	●			SDAD001B
			●						SDLD001A
	'653				●				·1B
			●						A
12-mA/24-mA/ 48-mA Sink, True and Inverting Output Transceivers	'644				A	●			SDAD001B
			●						SDLD001A
Registered with Multiplexed 12-mA/24-mA/ 48-mA True Output Transceivers	'647				A	●			SDAD001B
			●						SDLD001A
	'654		●						SDLD001A
					●				SDVD001
Registered with Multiplexed 12-mA/24-mA/ 48-mA Inverting Output Transceivers	'649		●						SDLD001A
					●				SDVD001

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY											LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	
Quad Buffers/ Drivers with Independent Output Controls	'125	●	A										·· ·A
								●					·B
	'126	●	A										)01A
								●					· ·)01B
Noninverting Octal Buffers/ Drivers	'241		●	●									SDLD001A
					B	●							SDAD001B
								●	●				SCLD001B
							●						SDFD001
												●	··
	'11241									●	●		· ·A
	'244		●	●									SDLD001A
					B	●							SDAD001B
								●	●				SCLD001B
							●						· · ·
												●	· · ·
	'11244									●	●		SCAD001A
	'465		●										SDLD001A
					A								SDAD001B
	'467				A								SDAD001B
			●										SDLD001A
	'541		●										·)01A
					●								·· ·001B
								●	●				SCLD001B
	'1244				A								SDAD001B

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

DRIVERS WITH 3-STATE OUTPUTS (continued)

DESCRIPTION	TYPE	TECHNOLOGY											LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	
Inverting Octal Buffers/Drivers	'231				●	●							SDAD001B
	'240		●	●									SDLD001A
					A	●							SDAD001B
								●	●				)001B
							●						)001
												●	004
	'11240									●	●		)001A
	'466		●										)001A
					A								)001B
	'468				A								SDAD001B
			●										SDLD001A
	'540		●										SDLD001A
					●								SDAD001B
								●	●				B
	'1240				●								1B
Inverting and Noninverting Octal Buffers/ Drivers	'230					●							SDAD001B
Noninverting 10-Bit Buffers/ Drivers	'2827											●	SCLS051
	'29827				●								SDVD001
												●	SCLS052
Inverting 10-Bit Buffers/Drivers	'2828											●	SCLS051
	'29828				●								SDVD001
												●	SCLS052

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY										LITERATURE NUMBER
		LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	
Noninverting Quad Transceivers	'243	●										SDLI
				A	●							SDAD001B
							●	●				SCLD001B
						●						SDFD001
Inverting Quad Transceivers	'242	●										SDLD001A
				B	●							SDAD001B
							●	●				SCLD001B
						●						SDFD001
	'1242			●								SDAD001B
Quad Tridirectional Transceivers	'442	●										SDLD001A
Octal Transceivers	'245	●										SDLD001A
				A	●							SDAD001B
							●	●				SCLD001B
						●						SDFD001
											▲	TBA
	'11245								●	●		SCAD001A
	'620						●	●				SCLD001B
				A	●							SDAD003
						●						SD
											●	SC
	'11620								▲	▲		SCAD001A
	'640						●	●				SCLD001B
				A	●							SDAD001B
		●										SDLD001A
	'11640								▲	●		SCAD001A
	'643						●	●				SCLD001B
				A	●							SDAD001B
		●										SDLD001A
	'11643								●	●		SCAD001A
	'1245			A								SDAD001A
											▲	TBA

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (continued)

DESCRIPTION	TYPE	TECHNOLOGY										LITERATURE NUMBER
		LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	
Octal Bus Transceivers with Registers	'543					●						SDFD001
	'544					●						SDFD001
	'646						●	●				SCL B
				●	●							SDA 1B
		●										SD A
	'648						●	●				SC B
				●	●							SD B
		●										SD A
	'651						●	●				SCLD001B
				●	●							SDAD001B
		●										SDLD001A
	'652						●	●				SCLD001B
				●	●							SDAD001B
		●										SDLD001A
	'11646								▲	▲		SCAD001A
	'11648								▲	▲		
	'11651								▲	▲		
	'11652								▲	▲		
8-/9-Bit Bus Transceivers with Parity Checker/ Generator	'658						●	●				SCLD001B
	'659						●	●				
	'664						●	●				
	'665						●	●				
	'29833			●								SDAS119A
											●	SCBS003
	'29834			●								SDAS119A
											●	SCBS003
	'29853			●								S118
											●	3002
	'29854			●								SDAS118
											●	SCBS002

● = Denotes available technology.
▲ = Denotes planned new
A = Denotes "A" suffix available in the technology indicated
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (continued)

DESCRIPTION	TYPE	TECHNOLOGY										LITERATURE NUMBER
		LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	
Noninverting 9-Bit Transceivers	'29863			●								SD iA
											●	SC
Inverting 9-Bit Transceivers	'29864			●								SDAS096A
											▲	TBA
Noninverting 10-Bit Transceivers	'29861			●								SDAS097
											●	SCLS056
Inverting 10-Bit Transceivers	'29862			●								SDAS097
											▲	TBA
12-mA/24-mA/48-mA Sink, True Output Transceivers	'623			A	●							SDAD001B
		●										SDLD001A
							●	●				SCLD001B
						●						)001
	'645						●	●				)001B
				A	●							1B
		●										A
	'654			●								SDAD001B
		●										SDLD001A
	'1640			A								SDAD001B
	'1645			A								
	'1								▲	▲		SCAD001A
Universal Transceiver/ Port Controllers	. '856				●							SDAD001B
	'877				●							

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

LINE DRIVERS/BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	BCT	
Bus Transceivers	'2242				●				SDAD001B
	'2243					●			
	'2244					●			
	'2640					●			
	'2645					●			
Line Drivers	'2240				●				
	'2240							▲	TBA
	'2241							▲	
	'2244				▲				
	'2244							▲	
	'2540				●				SDAD001B
	'2541				●				

LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Octal Buffers	'746				●				SDAD001B
AND/Line Drivers with Input Pull up Resistors	'747				●				
Octal/Line Drivers with 3-State Output	'2540				●				
	'2541				●				

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Quad 2-Input Positive-NOR	'128	●							SDLD001A
Dual 4-Input Positive-NAND	'140			●					
Hex 2-Input Positive-NAND	'804				A	B			SDAD001B
							●		SCLD001B
	'1804				A	●			SDAD001B
Hex 2-Input Positive-NOR	'805				A	B			
							●		SCLD001B
	'1805				A	●			SDAD001B
Hex 2-Input Positive-AND	'808				A	B			
							●		SCLD001B
	'1808				A	●			SDAD001B
Hex 2-Input Positive-OR	'832				A	B			
							●		SCLD001B
	'1832				A	●			SDAD001B

MULTIFUNCTION DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Dual Pulse Synchronizers/ Drivers	'120	●							SDLD001A

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY									LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	AC	ACT	F	
Dual J-K Edge-Triggered	'73	●	A								SDLD001A
							●				SCLD001B
	'76	●	A								SDLD001A
							●				SCLD001B
	'78	●	A								SDLD001A
							●				SCLD001B
	'107	●	A								SDLD001A
							●				SCLD001B
	'109	●	A								SDLD001A
					A	●					SDAD001B
							●				SCLD001B
										●	SDFD001
	'112		A	A							SDLD001A
					A						SDAD001B
							●				SCLD001B
										●	SDFD001
	'113		A	A							SDLD001A
					A						SDAD001B
							●				SCLD001B
										●	SDFD001
	'114		A	A							SDLD001A
					A						SDAD001B
							●				SCLD001B
										●	SDFD001
	'11109							●	●		SCAD001A
Single J-K Edge-Triggered	'70	●									SDLD001A
Dual D-Type	'74	●	A	●							SDLD001A
					A	●					SDAD001B
							●				SCLD001B
										●	SDFD001
	'11074							●	●		SCAD001A
Dual D-Type with 2-Input NAND/NOR Gates	'7074						●				SCLD001B
	'7075						●				
	'7076						●				
Dual 4-Bit D-Type Edge-Triggered	'874				B	●					SDAD001B
	'876				A	●					
	'878				A	●					
	'879				A	●					

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	OUTPUTS	NO. OF FFs	TYPE	TECHNOLOGY							LITERATURE NUMBER
				STD TTL	LS	S	ALS	AS	HC	F	
D-Type	Q, $\overline{Q}$	4	'175	●	●	●					SDLD001A
							●	●			SDAD001B
									●		SCLD001B
										●	SDFD001
			'379		●						SDLD001A
									●		SCLD001B
										●	SDFD001
	Q	6	'174	●	●	●					SDLD001A
							●	●			SDAD001B
									●		SCLD001B
										●	SDFD001
			'378		●						$\overline{SD}$ A
									●		SC $\overline{B}$
										●	SDFD001
J-K	Q	4	'276	●							SDLD001A
			'279	●	A						
			'376	●							

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY											LITERATURE NUMBER
				STD	LS	S	ALS	AS	HC	HCT	AC	ACT	BCT	F	
True Data	Octal	3-State	'374		●	●									SDLD001A
							●	●							SDAD001B
									●	●					SCLD001B
													▲		TBA
														●	SDFD001
			'574				A	●							SDAD001B
									●	●					SCLD001B
														●	SDFD001
			'11374								●	●			SDAD001A
True Data with Clear		2-State	'273	●	●										SDLD001A
							●								SDAD001B
									●						SCLD001B
														●	SDFD001
		3-State	'575				A	●							SDAD001B
			'874				A	●							
			'878				A	●							
True with Enable		2-State	'377		●										SDLD001A
									●						SCLD001B
														●	SDFD001
Inverting		3-State	'534				●	●							SDAD001B
									●	●					SCLD001B
													▲		TBA
														●	SDFD001
			'564				A								SDAD001B
									●	●					SCLD001B
														●	SDFD001
			'576				A	●							SDAD001B
			'826					●							SDAD001B
			'11534								●	●			SCAD001A
Inverting with Clear		3-State	'577				A	●							SDAD001B
			'879				A	●							
Inverting with Preset		3-State	'876				A	●							
True			'825					●							SDAD001B
	9-Bit	3-State	'823				●	●							
			'1823					●							SDAS126
Inverting		3-State	'824					●							SDAD001B
True	10-Bit	3-State	'821					●							
			'1821					●							SDAS131
Inverting		3-State	'822					●							SDAD001B

● = Denotes available technology.
▲ = Denotes planned new
A = Denotes "A" suffix available in the technology indicated
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

LATCHES AND MULTIVIBRATORS

QUAD LATCHES WITH 2-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Bistable	'75	●	●						SDL A
							●		SC B
	'375		●						SDLD001A
							●		SCLD001B
S-R	'279	●	A						SDLD001A

MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
Single	'121	●							SDLD001A
		●	●						
		●							
Dual	'123	●	●						
	'221	●	●						
	'423		●						

D-TYPE OCTAL, 9-BIT, AND 10-BIT READ-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY							LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	HCT	
Edge-Triggered Inverting and Noninverting	Octal	'996				●				SDAD001B
Transparent True	Octal	'990				●				
	9-Bit					●				
	10-Bit	[illegible]				●				
Transparent Noninverting	Octal	'991				●				
	9-Bit	'993				●				
	10-Bit	'995				●				
Transparent with Clear and True Outputs	Octal	'666				●				
Transparent with Clear and Inverting Outputs	Octal	'667				●				

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY											LITERATURE NUMBER
				STD TTL	LS	S	ALS	AS	HC	HCT	AC	ACT	BCT	F	
Transparent	Octal	3-State	'373		●	●									SDLD001A
							●	●							SDAD001B
									●	●					SCLD001B
													▲		TBA
														●	SDFD001
			'573				B	●							1B
									●	●					B
														●	SDFD001
			'11373								●	●			SCAD001A
Dual 4-Bit Transparent	Octal	2-State	'116	●											SDLD001A
		3-State	'873				B	●							SDAD001B
Inverting Transparent	Octal	3-State	'533				●	●							SDAD001B
									●	●					SCLD001B
													▲		TBA
														●	SDFD001
			'11533								●	●			SCAD001A
			'563				A								01B
									●	●					SCLD001B
														●	SDFD001
			'580				A	●							SDAD001B
Dual 4-Bit Inverting Transparent	Octal	3-State	'880				A	●							
2-Input Multiplexed	Octal	3-State	'604		●										SDLD001A
									●						SCLD001B
		OC	'607		●										SDLD001A
Addressable	Octal	2-State	'259	●	B										
							●								1B
									●						1B
		Q only	'4724						●						SCLD001B
True	10-Bit	3-State	'841				●	●							SDAD001B
			'1841					●							SDAS130
True	9-Bit	3-State	'843				●	●							SDAD001B
			'1843					●							SDAS127
True	Octal	3-State	'845				●	●							SDAD001B
Inverting	10-Bit	3-State	'842				●	●							
	9-Bit	3-State	'844				●	●							
	Octal	3-State	'846				●	●							

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced*

REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY							LITERATURE NUMBER
		S-	S	L	H		STD TTL	LS	S	ALS	AS	HC	F	
Sign-Protected		X		X	X	'322		A						SDLD001A
Parallel-In Parallel-Out Bidirectional	4	X	X	X	X	'194	●	A	●					SD[illegible] A
											●			SD[illegible] B
												●		SCLD001B
	8	X	X	X	X	'198	●							SDLD001A
		X	X	X	X	'299		●						S[illegible]001A
										●				S[illegible]1B
												●		SC[illegible]1B
													●	SDFD001
		X	X	X	X	'323		●						SDLD001A
										●				[illegible]B
												●		[illegible]B
													●	[illegible]0001
Parallel-In Parallel-Out	4	X		X		'95	A	B						[illegible]001A
											●			[illegible]B
		X		X		'195	●	●	●					SD[illegible]A
												●		SC[illegible]B
		X		X		'295		B						SDLD001A
		X		X		'395		A						
	5	X		X		'96	●	●						
	8	X		X	X	'199	●							
Serial-In Parallel-Out	8	X				'164	●	●						[illegible]A
												●		[illegible]B
Parallel-In Serial-Out	8	X		X	X	'165	●	A						[illegible]0001A
												●		[illegible]0001B
		X		X	X	'166	●	A						[illegible]0001A
												●		[illegible]0018
	16	X		X	X	'674		●						
Serial In Serial-Out	8	X				'91		●						SDLD001A

NOTE: Modes: S- = S R, S = S-L, L = Load, H = Hold

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced*

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY						LITERATURE NUMBER
				STD TTL	LS	S	ALS	AS	HC	
Parallel-In, Parallel-Out with Output Latches	4	3-State	'671		●					SDLD001A
			'672		●					
Serial-In Parallel-Out with Output Latches	8	Buffered	'594		●					SDLD001A
									●	B
		3-State	'595		●					A
					●					SCLD001B
		OC	'599		●					
	16	2-State	'673		●					
Parallel-In, Serial-Out with Input Latches	8	2-State	'597		●					SDLD001A
Parallel I/O Ports with Input Latches Multiplexed Serial Inputs	8	3-State	'598		●					

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES				TYPE	TECHNOLOGY						LITERATURE NUMBER
		S-	S	L	H		STD TTL	LS	S	ALS	AS	HC	
Sign-Protected Registers	8	X		X	X	'322		A					SDLD001A

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	
Dual 16 Words X 4 Bits	3-State	'870				▲	●		SDAD001B
		'871				▲	●		
4 Words X 4 Bits	OC	'170	●	●					SDLD001A
	3-State	'670		●					
8 Words X 2 Bits	3-State	'172	●						
64 Words X 40 Bits	3-State	'8834					▲		TBA

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	BCT	
Quadruple Multiplexers with Storage	'298	●	●						SDLD001A
						●			SDAD001B
							●		SCLD001B
8-Bit Universal Shift Registers	'299		●						SDLD001A
					●	●			SDAD001B
Quadruple Bus Buffer Register	'173	●	A						SDLD001A
							●		SCLD001B
Data Selector/ Multiplexer/ Register	'356		●						SDLD001A
							●		SCLD001B
Dual-Rank 8-Bit Shift Register	'963				▲				SDVD001
	'964				▲				
8-Bit Diagnostic/ Pipeline Register	'819				●				SDAS105
	'29818				●				
								▲	TBA

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

COUNTERS

SYNCHRONOUS COUNTERS — POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	F	
Decade	Sync	'160	●	A						SDL 'A
						B	●			SD 'B
								●		B
									●	
		'162	●	A	●					SDLD001A
						B	●			SDAD001B
								●		SCLD001B
									●	SDFD001
		'560				A				SDAD001B
		'692		●						SDLD001A
Decade Up/Down	Sync	'168				B	●			SDAD001B
									●	SDFD001
	Async	'190	●	●						SDLD001A
						●				SDAD001B
								●		SCLD001B
		'192	●	●						SDLD001A
						●				SDAD001B
								●		SCLD001B
	Sync	'568				A				SDAD001B
									●	SDFD001
		'696		●				▲		SDLD001A
4-Bit Binary	Sync	'161	●	A						SDLD001A
						B	●			SD 'B
								●		SC B
									●	SDI
		'163	●	A						SDI A
						B	●			SDAD001B
								●		SCLD001B
									●	SDI
		'561				A				SD 'B
		' ' '		●						SDLD001A
				●						SDLD001A
		'693		●						SDLD001A
		'8161				●				SDAS116
		'8163				●				SDAS104

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SYNCHRONOUS COUNTERS — POSITIVE-EDGE TRIGGERED (continued)

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	F	
4-Bit Binary Up/Down	Async	'191	●	●						SDI IA
						●				SDAS001B
								●		SCLD001B
		'193	●	●						001A
						●				SDAS001B
								●		SCLD001B
	Sync	'169		B	●					SDLD001A
						B	●			SDAS001B
									●	001
		'569				A				SDAS001B
									●	SDFD001
		'697		●						SDLD001A
		'699		●						
		'8169				●				SDAS117
8-Bit Up/Down	Async CLR	'867				●	●			SDVD001
	Sync CLR	'869				●	●			
Divide-By-10 Johnson Counter		'4017						●		SCLD001B
Divide-By-8 Johnson Counter		'7022						●		

● ≡ Denotes available technology.
▲ ≡ Denotes planned new
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) — NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	
Decade	Set-to-9	'90	A	●					SDLD001A
	Yes	'176	●						
	Yes	'196	●	●	●				
	Set-to-9	'[illegible]	A	●					
4-Bit Binary	None	'[illegible]	A	A					
	Yes	'177	●						
	Yes	'197	●	●	●				
Divide-By-12 Dual Decade	None	'[illegible]	●	●					
		'[illegible]	A	●					
		'390	●	●					SDLD001A
								●	[illegible]D001B
	Set-to-9	'490						●	[illegible]D001B
			●	●					D001A
Dual 4-Bit Binary	None	'393	●	●					D001A
								●	SCLD001B
7-Bit Binary		'4024						●	SCLD001B
12-Bit Binary		'4040						●	
14-Bit Binary		'4020						●	
		'4060						●	
		'4061						●	

● ≡ Denotes available technology.
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated.
B ≡ Denotes "B" suffix available in the technology indicated.
TBA ≡ Denotes information *To Be Announced.*

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						LITERATURE NUMBER
			STD TTL	LS	S	ALS	AS	HC	
Parallel Register Outputs	3-State	'590		●					SDLD001A
								●	SCLD001B
	OC	'591		●					SDLD001A
Parallel Register Inputs	2-State	'592		●					
Parallel I/O	3-State	'593		●					

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY							LITERATURE NUMBER
		STD TTL	LS	S	ALS	AS	HC	HCT	
60-Bit Binary Rate Multiplier	'97	●							SDLD001A
Decade Rate Multiplier	'167	●							
Programable Frequency Dividers/Digital Timers	'282					●			SDAD001B
	'284		●						SDLD001A

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

PROGRAMMABLE LOGIC ARRAYS

STANDARD HIGH-SPEED PAL® CIRCUITS (ALS)

TYPE	INPUTS	OUTPUTS		NO. OF PINS	PACKAGES	LITERATURE NUMBER
		NO.	TYPE			
PAL16L8A	16	8	Active Low	20	FK,FN,J,N	SDZD001B
PAL16R4A		4	Registered			
PAL16R6A		6				
PAL16R8A		8				
PAL16L8A-2		8	Active Low			
PAL16R4A-2		4	Registered			
PAL16R6A-2		6				
PAL16R8A-2		8				
PAL20L8A	20	8	Active Low	24	FK,FN,JT,NT	
PAL20R4A		4	Registered			
PAL20R6A		6				
PAL20R8A		8				
PAL20L8A-2		8	Active Low			
PAL20R4A-2		4	Registered			
PAL20R6A-2		6				
PAL20R8A-2		8				

HIGH PERFORMANCE PAL® CIRCUITS (ALS)

TYPE	INPUTS	OUTPUTS		NO. OF PINS	PACKAGES	LITERATURE NUMBER
		NO.	TYPE			
TIBPAL16L8-10	16	8	Active High	20	FK,FN,J,N	SDZD001B
TIBPAL16R4-10		4	Register			
TIBPAL16R6-10		6				
TIBPAL16R8-10		8				
TIBPAL16L8-12		8	Active High			
TIBPAL16R4-12		4	Register			
TIBPAL16R6-12		6				
TIBPAL16R8-12		8				
TIBPAL16H8-15			Active High			TBA
TIBPAL16HD8-15						
TIBPAL16L8-15			Active Low			SDZD001B
TIBPAL16HD8-15						TBA
TIBPAL16R4-15		4	Registered			SDZD001B
TIBPAL16R6-15		6				
TIBPAL16R8-15		8				
TIBPAL16H8-25		8	Active High			TBA
TIBPAL16HD8-25						
TIBPAL16L8-25		8	Active Low			SDZD001C
TIBPAL16LD8-25						

● ≡ Denotes available technology
▲ ≡ Denotes planned new.
A ≡ Denotes "A" suffix available in the technology indicated
B ≡ Denotes "B" suffix available in the technology indicated
TBA ≡ Denotes information *To Be Announced*

PAL is a registered trademark of Monolithic Memories Inc.

HIGH PERFORMANCE PAL® CIRCUITS (ALS) (continued)

TYPE	INPUTS	OUTPUTS		NO. OF PINS	PACKAGES	LITERATURE NUMBER
		NO.	TYPE			
TIBPAL16R4-25	16	4	Registered	20	FK,FN,J,N	SDZD001B
TIBPAL16R6-25		6				
TIBPAL16R8-25		8				
TIBPAL16L8-30		8	Active Low			
TIBPAL16R4-30		4	Registered			
TIBPAL16R6-30		6				
TIBPAL16R8-30		8				
TIBPAL20L8-15	20	8	Active Low	24	FK,FN,JT,NT	SDZD001B
TIBPAL20R4-15		4	Registered			
TIBPAL20R6-15		6				
TIBPAL20R8-15		8				
TIBPAL20L8-25		8	Active Low			
TIBPAL20R4-25		4	Registered			
TIBPAL20R6-25		6				
TIBPAL20R8-25		8				
TIBPAL20L8-20		10	Active Low			
TIBPAL20R4-20		4	Registered			
TIBPAL20R6-20		8				
TIBPAL20R8-20		10				
TIBPAL20L8-30		10	Active Low			TBA
TIBPAL20R4-30		4	Registered			
TIBPAL20R6-30		8				
TIBPAL20R8-30		10				
TIBPALR19L8	19	8	Active Low			SDZD001B
TIBPALR19R4		4	Registered			
TIBPALR19R6		6				
TIBPALR19R8		8				
TIBPALT19L8		8	Active Low			
TIBPALT19R4		4	Registered			
TIBPALT19R6		6				
TIBPALT19R8		8				

HIGH PERFORMANCE CMOS PAL® CIRCUITS

TYPE	INPUTS	OUTPUTS		NO. OF PINS	PACKAGES	LITERATURE NUMBER
		NO.	TYPE			
TICPAL16L8-55	16	8	Active High	20	JL,N	TBA
TICPAL16R4-55		4	Register			
TICPAL16R6-55		6				
TICPAL16R8-55		8				

● = Denotes available technology.
▲ = Denotes planned new
A = Denotes "A" suffix available in the technology indicated.
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

PAL is a registered trademark of Monolithic Memories Inc

HIGH PERFORMANCE IMPACT PROGRAMMABLE ARRAY LOGIC

TYPE	INPUTS	OUTPUTS		NO. OF PINS	PACKAGES	LITERATURE NUMBER
		NO	TYPE			
TIBPAL22V10	12 Inputs or 11 Inputs with CLK	10	I/O	24	NT,FN	SDPS015
AL22V10A						
AL22V10A						SDPS106

FIELD PROGRAMMABLE LOGIC ARRAY (ALS)

TYPE	INPUTS	OUTPUTS		NO. OF PINS	ARRAY	PACKAGES	LITERATURE NUMBER
		NO.	TYPE				
TIFPLA839	14	6	3-State	24	14×32×6	FK,FN,N,NT	SDZD001A
TIFPLA840			OC				
TIB82S167B			3-State		14×48×6		
67A							
2S105B	16	8	3-State	28		FK,FN,JD,N	
05A			3-State				

BIPOLAR MEMORY

FIRST-IN FIRST-OUT MEMORIES (FIFOs)

DESCRIPTION	TYPE OF	TYPE	TECHNOLOGY							PACKAGES	LITERATURE NUMBER
			STD TTL	ALS	AS	LS	S	HC	HCT		
16 Words×4 Bits	3-State					●				J,N	SDVD001
	3-State					●					
	3-State			A						D,N,FK,FN	
	OC					●				J,N	
	OC					●					
16 Words×5 Bits	3-State						●			J,N	
	3-State	'229		A						DW,FK,FN	
	3-State	'234		●						DW,J,FK,FN	SDAS106
	3-State			A						DW,FK,FN,J,N	SDVD001
64 Words×4 Bits	3-State			●						DW,J,FK,FN	SDAS107
64 Words×5 Bits	3-State	'235		●						DW,FN,FK,N	SDAS108

● = Denotes available technology.
▲ = Denotes planned new.
A = Denotes "A" suffix available in the technology indicated
B = Denotes "B" suffix available in the technology indicated.
TBA = Denotes information *To Be Announced.*

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

*Current out of a terminal is given as a negative value

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_f **Fall time**
The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or  , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

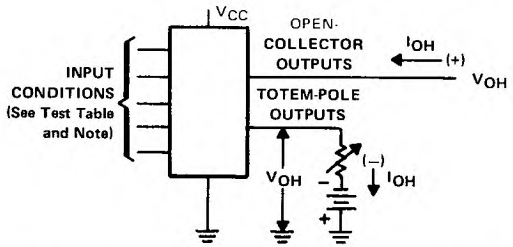
The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. The entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

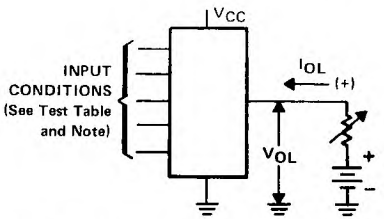


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR INVERT	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, I_{OH}

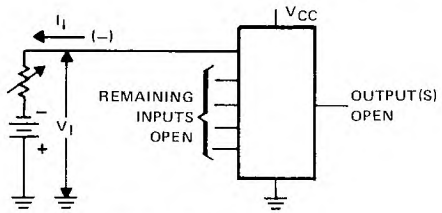


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR-INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

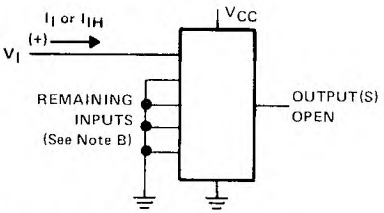
NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 2. V_{IH}, V_{IL}, V_{OL}



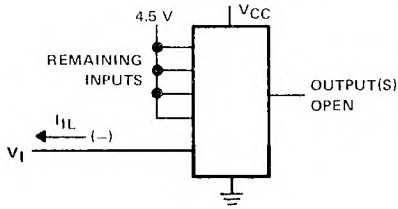
NOTE: Each input is tested separately.

FIGURE 3. V_I



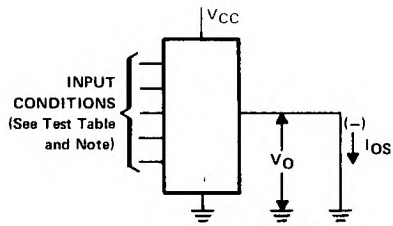
NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_I and grounded when testing I_{IH}

FIGURE 4. I_I, I_{IH}



NOTES. A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with input of AND gates not under test open.

FIGURE 5. I_{IL}

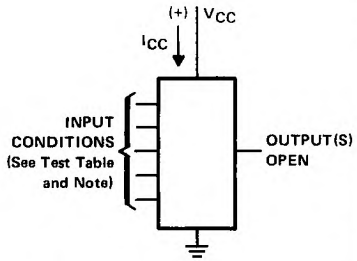


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at [illegible]
AND-OR	All inputs at [illegible]

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 6. I_{OS}, I_O



TEST TABLE

FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4 5 V, all others at GND	All inputs at GND

NOTE: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations.:

$$I_{CC}, I_{CCH}, \text{ or } I_{CCL} \text{ (average per gate or flip-flop)} = \frac{\text{total } I_{CC}, I_{CCH}, \text{ or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC} \text{ (average per gate, 50\% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2 \text{ (number of gates in package)}}$$

FIGURE 7. I_{CC}

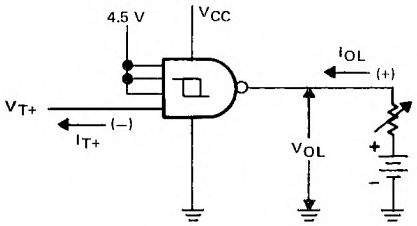


FIGURE 8. V_{T+}, I_{T+}, V_{OL}
(FOR NAND SCHMITT TRIGGERS)

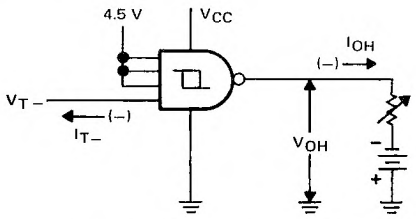
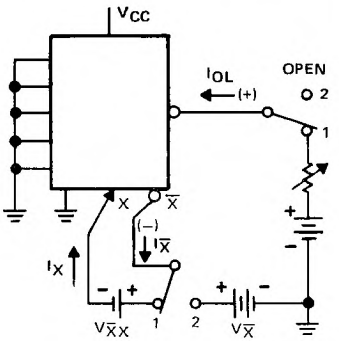


FIGURE 9. V_{T-}, I_{T-}, V_{OH}
(FOR NAND SCHMITT TRIGGERS)



NOTES: A. Switches are in position 1 for SN54'/SN74'
B. The $I_{\overline{X}}$ limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The $V_{\overline{X}X}$ source is replaced by a resistor (see table below) in parallel with a voltmeter between the X and $\overline{X}$ pins. If the measured voltage, V_{XX}, is less than 0.4, the specified limit for $I_{\overline{X}}$ is met.

RESISTANCE VALUE TABLE

SN5423	114 Ω
SN5450, SN5453	138 Ω
SN7423	105 Ω
SN7450, SN7453	130 Ω

FIGURE 10. I_X (FOR EXPANDABLE GATES)

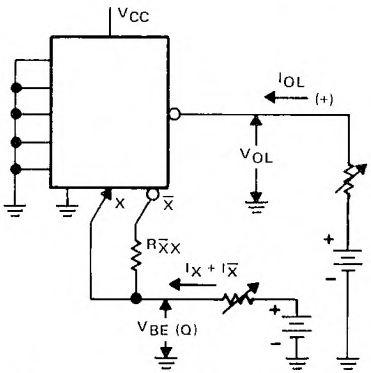


FIGURE 11. $V_{BE(Q)}$ (FOR EXPANDABLE GATES)

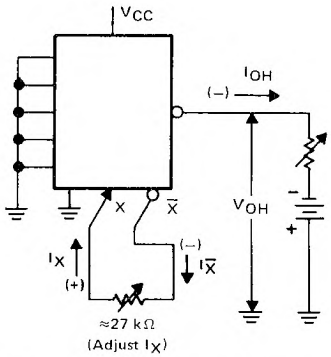


FIGURE 12. V_{OH} (FOR EXPANDABLE GATES)

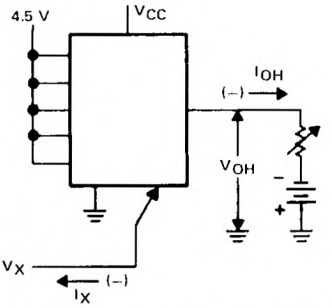


FIGURE 13. V_{OH} (FOR EXPANDABLE GATES)

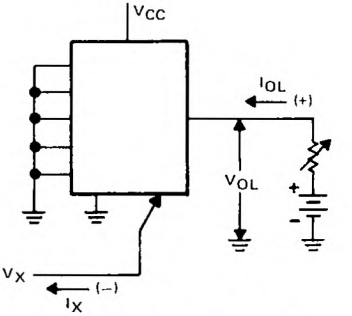


FIGURE 14. V_{OL} (FOR EXPANDABLE GATES)

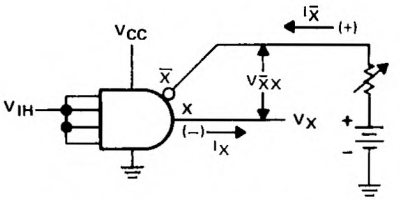


FIGURE 15. ON-STATE CHARACTERISTICS FOR EXPANDERS

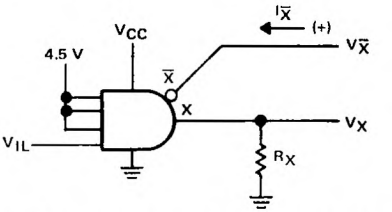


FIGURE 16. OFF-STATE CHARACTERISTICS FOR EXPANDERS

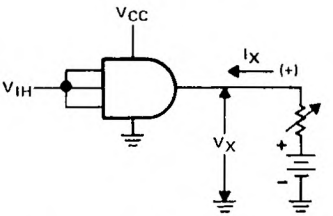


FIGURE 17. ON-STATE CHARACTERISTICS FOR EXPANDERS

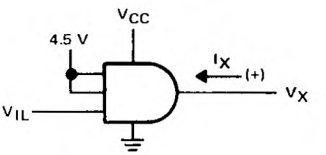


FIGURE 18. OFF-STATE CHARACTERISTICS FOR EXPANDERS

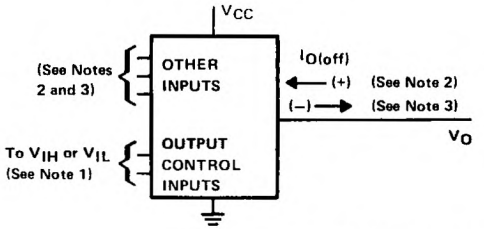
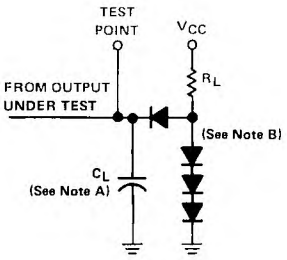


FIGURE 19. $I_{O(off)}$ (THREE-STATE OUTPUTS)

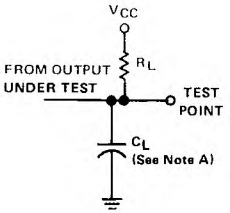
NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

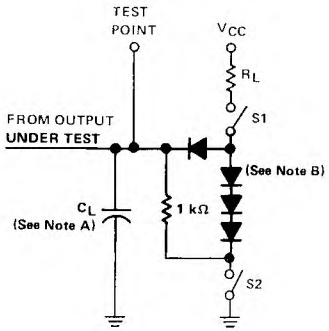
SERIES 54/74 and 54S/74S



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

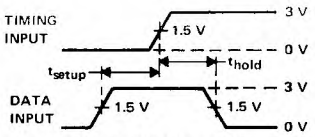


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

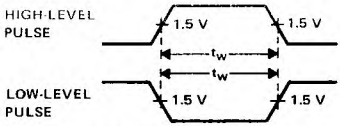


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

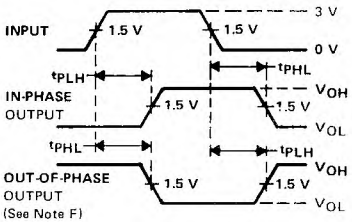
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent



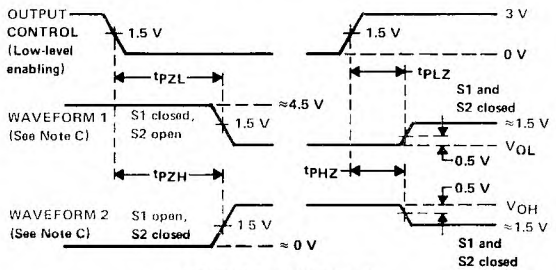
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



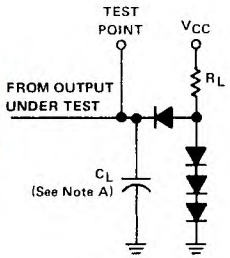
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



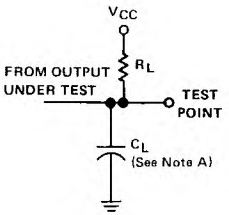
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω and:
For Series 54/74, t_r ≤ 7 ns, t_f ≤ 7 ns.
For Series 54S/74S, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. The outputs are measured one at a time with one input transition per measurement.

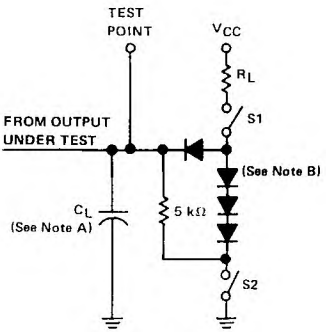
SERIES 54LS/74LS



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

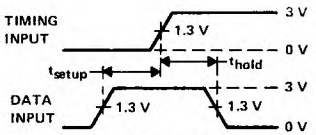


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

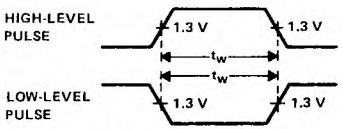


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

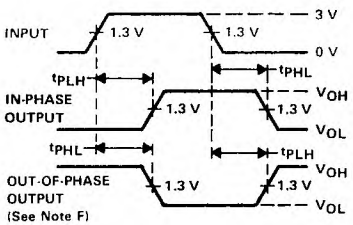
NOTES: A. C_L includes probe and jig capacitance
B. All diodes are 1N3064 or equivalent.



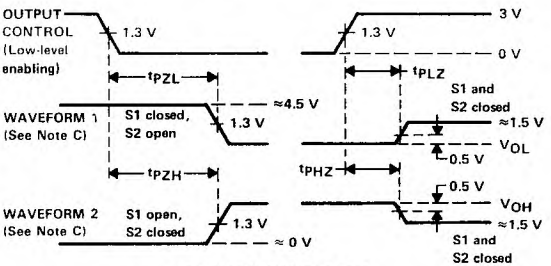
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω and for Series 54LS/74LS, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. The outputs are measured one at a time with one input transition per measurement.

SERIES 54/74†

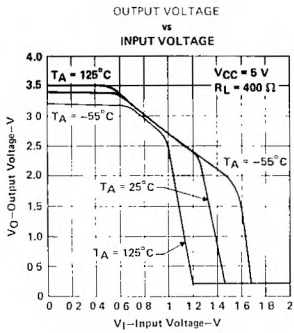


FIGURE A1

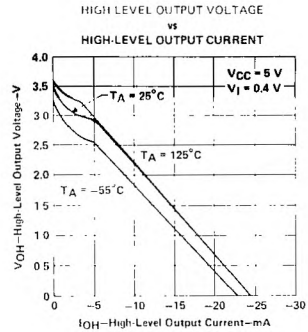


FIGURE A2

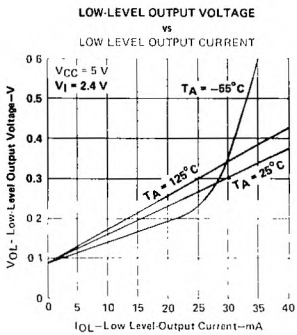


FIGURE A3

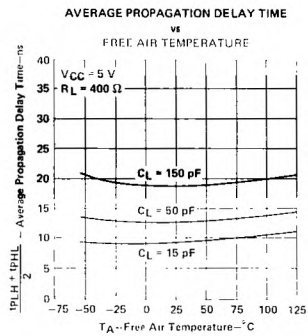


FIGURE A4

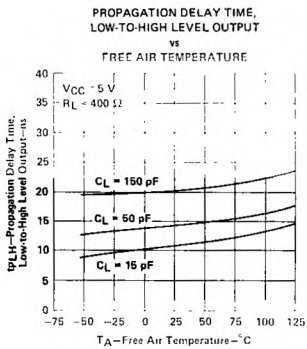


FIGURE A5

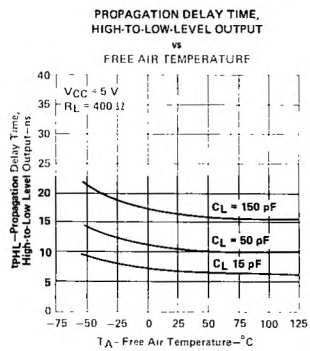


FIGURE A6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

SERIES 54LS/74LS†

OUTPUT VOLTAGE vs INPUT VOLTAGE (DIODE INPUT)

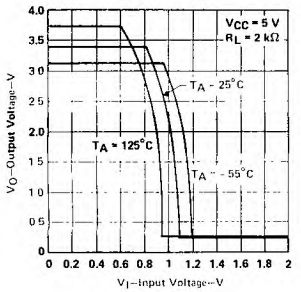


FIGURE D1

OUTPUT VOLTAGE vs INPUT VOLTAGE (PNP INPUT)

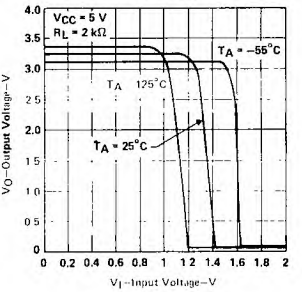


FIGURE D2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT (STANDARD OUTPUT)

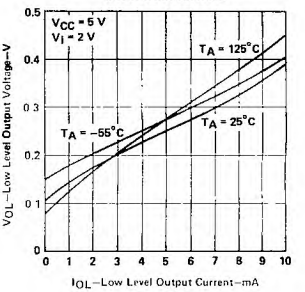


FIGURE D3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT (BUFFER OUTPUT)

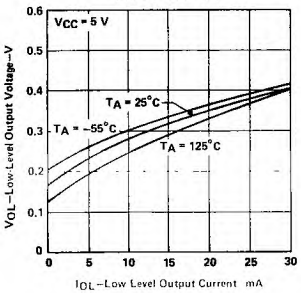


FIGURE D4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

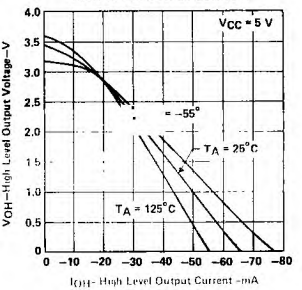


FIGURE D5

POWER DISSIPATION PER GATE vs FREQUENCY

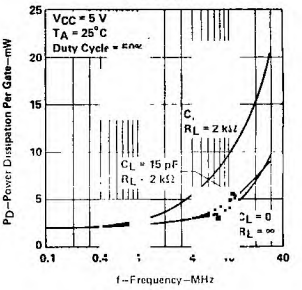


FIGURE D6

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

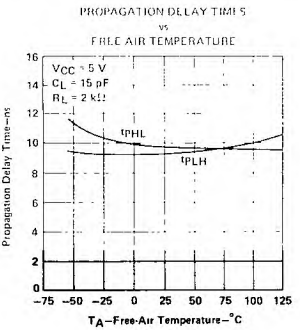


FIGURE D7

PROPAGATION DELAY TIMES vs LOAD CAPACITANCE

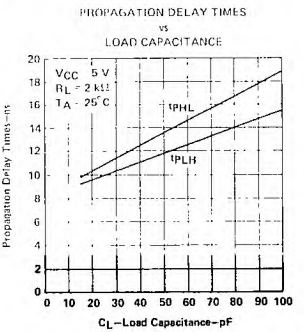


FIGURE D8

†Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.

SERIES 54S/74S†

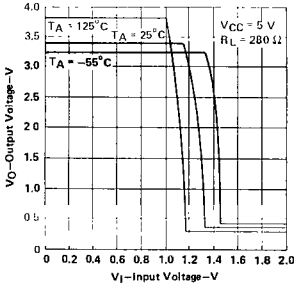


FIGURE E1

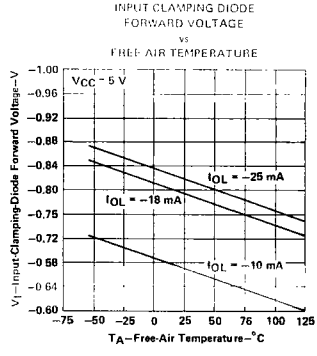


FIGURE E2

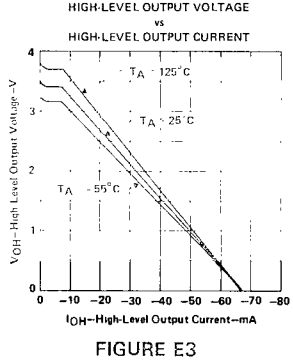


FIGURE E3

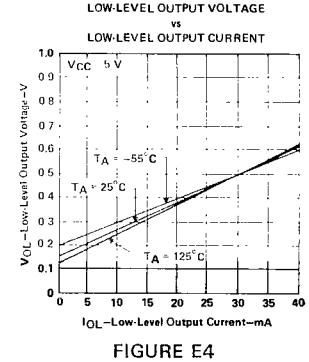


FIGURE E4

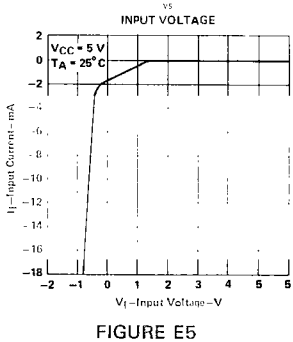


FIGURE E5

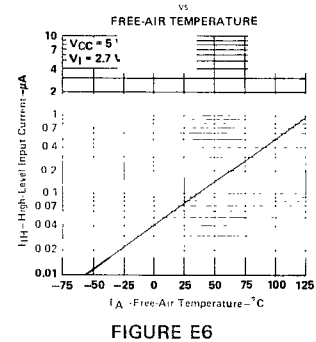


FIGURE E6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

SERIES 54S/74S†

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

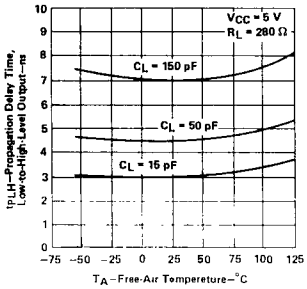


FIGURE E7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

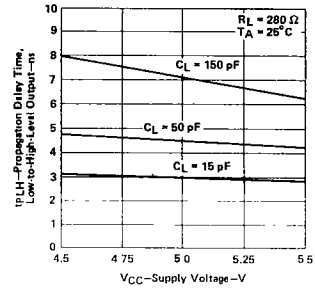


FIGURE E8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

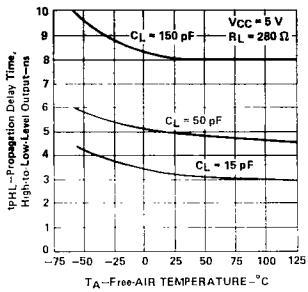


FIGURE E9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

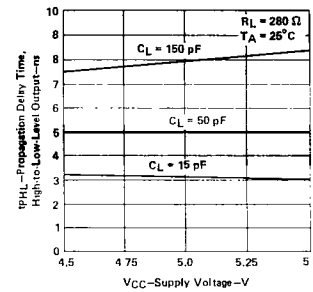


FIGURE E10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

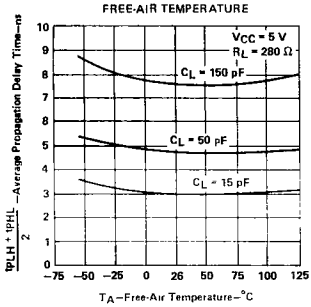


FIGURE E11

POWER DISSIPATION PER GATE
vs
FREQUENCY

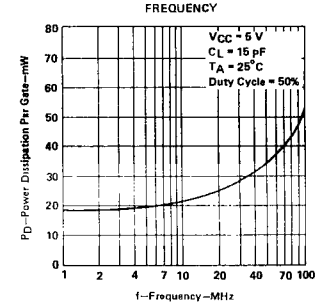


FIGURE E12

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SERIES 54S/74S†

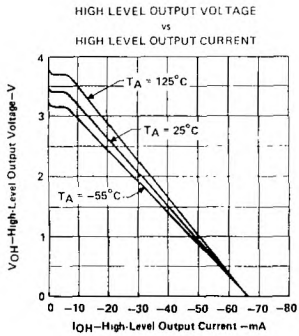


FIGURE E13

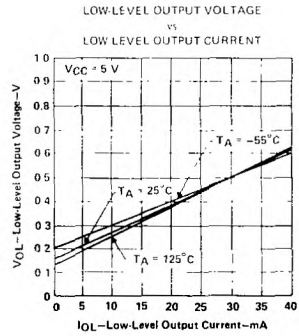


FIGURE E14

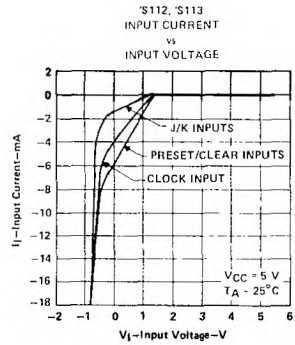


FIGURE E15

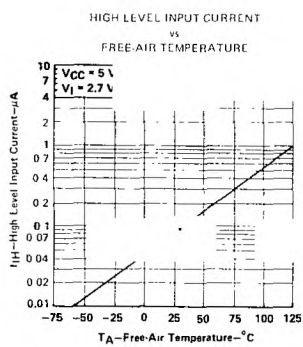


FIGURE E16

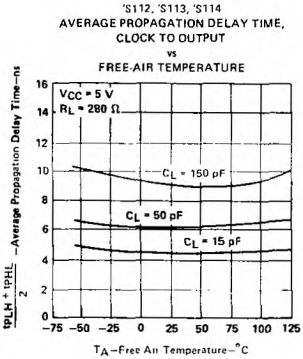


FIGURE E17

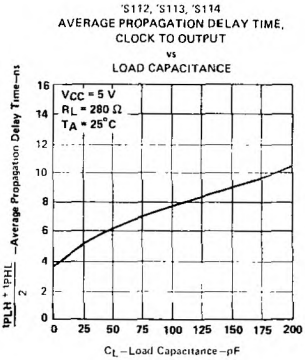


FIGURE E18

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.